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DESIGN OF A RELIABLE POWER SUPPLY SYSTEM FOR IOT TERMINALS IN HARSH ENVIRONMENTS

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Abstract
To address communication interruptions and low energy efficiency caused by inadequate power-supply dynamic response in Internet of Things (IoT) terminals operating in harsh environments, this study proposes and implements a power supply system based on dynamic voltage regulation via an operational-amplifier (op-amp) adder. The system innovatively modifies the feedback network of a conventional switching power supply: an analog voltage output from the MCU's digital-to-analog converter (DAC) is summed with a fixed reference voltage to dynamically configure the feedback reference potential of a BUCK converter, thereby enabling continuous, high-precision regulation of the output voltage. A software algorithm dynamically computes and outputs the corresponding DAC value according to the real-time sleep, standby, and transmit states of the cellular module, allowing the supply voltage to adaptively switch between a minimum baseline voltage and a maximum allowable voltage. The voltage is lowered in low-power states to save energy, and raised before high-power transmission to optimize power-amplifier efficiency and prevent system crashes caused by line voltage drop. Experimental results show that the system effectively eliminates system restarts caused by power-supply droop and improves overall energy efficiency over a typical duty cycle, significantly enhancing device reliability and endurance under harsh power-supply conditions.

1. Introduction
With the widespread adoption of IoT technology in smart agriculture, industrial monitoring, remote control, and similar applications, large numbers of terminal devices must be deployed outdoors or on industrial sites with harsh power-supply conditions, relying on batteries, solar power, and similar energy sources. Cellular communication modules exhibit highly dynamic current characteristics during operation, ranging from microampere-level sleep currents to ampere-level transmit currents; such abrupt load variation poses a severe challenge to the dynamic response and reliable operation of the power supply system[1], [2], [3], [4].

Existing power supply systems mostly use fixed-output-voltage BUCK converters or battery power directly. The former sets the output voltage to a typical value for the cellular module (e.g., 3.8 V); its advantage is circuit simplicity, but it cannot adapt to dynamic load variation, under high-current conditions the output voltage droops, potentially causing the module to reset owing to undervoltage. A fixed voltage also cannot match the cellular module's optimal efficiency point across different output power levels, resulting in energy loss[5], [6]. Battery

power simplifies the supply architecture but is constrained by the discharge curve: battery voltage declines with load and remaining capacity, reliability issues are prominent, and there is no active voltage-regulation capability to optimize overall energy efficiency.

To address these shortcomings, this paper proposes a coordinated dynamic-voltage-regulation scheme based on an op-amp adder and a controller. The scheme modifies the feedback network of a conventional switching power supply by introducing an adder circuit composed of the controller's DAC output and a fixed reference voltage, thereby enabling continuous, precise regulation of the BUCK converter's output voltage. Based on the real-time module state (sleep, standby, or transmit) it acquires, the system software dynamically adjusts the optimal target voltage[7], [8], lowering the voltage in low-power states to reduce static power loss, and raising it in anticipation of high-current transmission to compensate for line voltage drop and optimize cellular-module efficiency[9], [10], [11], thereby ensuring communication reliability, maximizing system energy efficiency, and extending the endurance of terminal devices in harsh environments.

2. System Architecture Design

The overall system design is shown in Fig. 1. The software–hardware co-designed dynamic-voltage-regulation architecture adopted in this work consists of three parts, a BUCK power supply module, an op-amp adder module, and a cellular communication module, which together form a complete functional loop from stable start-up to intelligent voltage regulation.

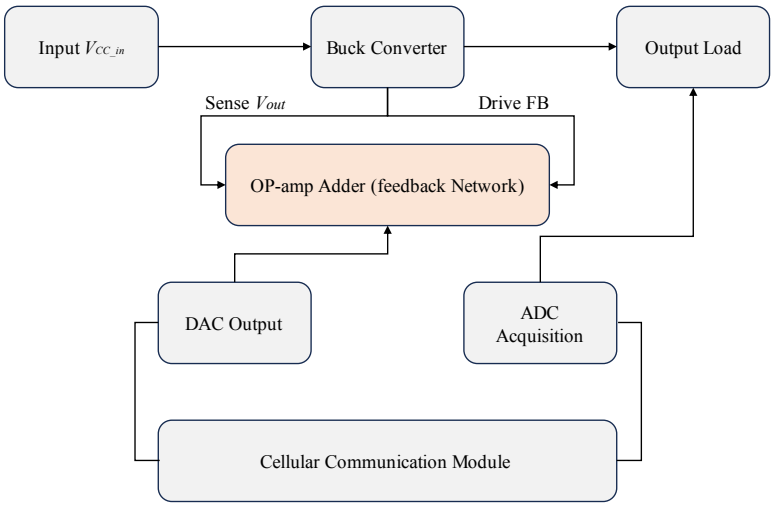

Fig. 1. Overall system block diagram

The BUCK power supply module serves as the system's basic power-supply unit, whose main function is voltage conversion and power delivery. It converts the front-end input voltage to the cellular module's operating voltage and provides the initial power for the entire voltage-regulation loop[12], [13].

The op-amp adder module is the hardware interface that enables dynamic voltage regulation. Its core function is to sum two analog signals: one from the resistor-divider network at the BUCK power supply's output, and the other from the cellular module's DAC output. During the initial power-up phase, the cellular module has not yet started and its DAC produces no output; at this point, the op-amp adder passes the BUCK power supply's default divided-down signal to its feedback pin, causing the BUCK power supply to output the highest default voltage set by the divider resistors, which starts up the cellular module[14], [15].

Once started, the cellular module acts as the controller and mainly performs two tasks: first, it uses its built-in ADC channel to sample the supply line voltage and current signals in real time, completing system operating-state monitoring; second, based on the algorithm's computed result, it outputs a high-precision analog control voltage via its DAC channel. This DAC output voltage is fed into the op-amp

adder circuit, where it is superimposed on the original divided-down signal; the resulting combined potential changes the reference voltage at the BUCK power supply's feedback pin, thereby linearly and continuously regulating the power supply's final output voltage and achieving a smooth reduction from the default maximum voltage to a lower target voltage.

3. Hardware Circuit Design

The overall hardware circuit design is shown in Fig. 2. The power supply circuit in this work is designed for a 5G NR module, with the power circuit built around three core objectives: meeting the module's 3–4 A transient peak-current requirement, achieving a wide (3.2–4.4 V) output-voltage range, and realizing intelligent dynamic voltage regulation. The main power-conversion IC is TI's synchronous BUCK converter TPS62903-Q1, chosen for its continuous output-current capability of up to 3 A, excellent transient response, and switching frequency of up to 2.25 MHz. To achieve precise, intelligent regulation of the output voltage, the system uses the rail-to-rail operational amplifier TLV9062 to form the adder circuit; its input and output ranges extend close to the supply rails, overcoming the inability of conventional op-amps to output near 0 V at low voltage and enabling wider, more linear feedback control.

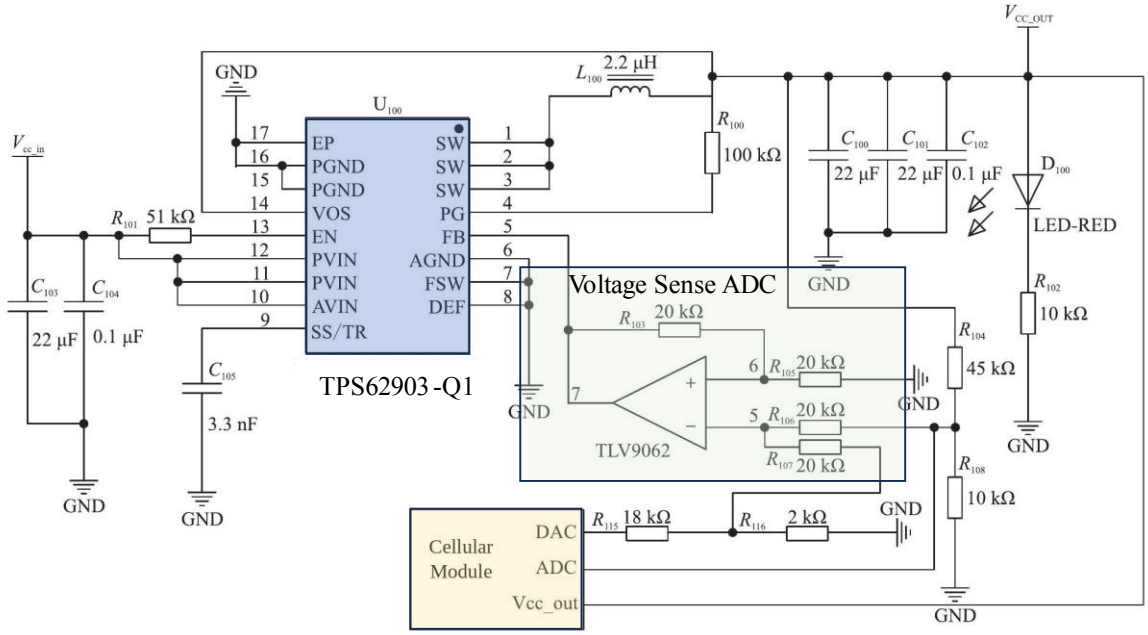

Fig. 2. Overall hardware circuit design

The circuit's voltage-regulation function is implemented by a resistor network together with the TLV9062 op-amp circuit. By default, before the module starts up, its DAC produces no output, and the output voltage V_out is set by resistors R104 (45 kΩ) and R108 (10 kΩ). Given the TPS62903-Q1's FB feedback reference voltage V_ref = 0.8 V, V_out = V_ref · (1 + R104/R108), yielding a default output of approximately 4.4 V, which ensures the output voltage never exceeds the maximum voltage the module can tolerate. Once the module starts up, its built-in DAC can output an analog voltage V_dac of 0–2 V. This voltage is attenuated by a divider formed by R115 (18 kΩ) and R116 (2 kΩ), so that the voltage actually delivered to the TLV9062's non-inverting input is V_in = V_dac · [R116/(R115+R116)] = V_dac/10. The TLV9062 is configured as a unity-gain voltage follower, giving an output V_opamp_out = V_in + V_out · [R108/(R108+R104)].

The key to voltage regulation is that the op-amp's output V_opamp_out is connected to the TPS62903-Q1's feedback pin (FB); V_opamp_out and the voltage at the FB pin are therefore equal, at 0.8 V. When the module's DAC outputs its maximum value of 2 V, V_in is 0.2 V, giving V_out ≈ 3.3 V; when the DAC output is 0 V, V_out returns to 4.4 V. By linearly controlling the DAC output in software, the output voltage can be precisely and continuously regulated over the 3.3–4.4 V range, matching

the module's optimal supply voltage under different operating states.

Regarding loop stability, the TLV9062 op-amp used in this work has a gain–bandwidth product of 10 MHz, far higher than the TPS62903-Q's 2.25 MHz switching frequency; the phase lag it introduces into the feedback loop is therefore negligible [10] and does not materially affect the phase margin of the original power-control loop, ensuring dynamic stability across the full regulation range.

Regarding the safety mechanism, if the module's DAC output state becomes indeterminate owing to a crash, runaway code, or a similar fault (e.g., the output latches, enters a high-impedance state, or jumps unpredictably), the resistor-divider network (R104, R108) together with the op-amp adder ensures that, regardless of the DAC's output state, the BUCK converter's maximum output voltage is limited to 4.4 V, below the module's maximum rated voltage, eliminating the risk of overvoltage damage.

The system software includes a built-in watchdog timer; if the main program hangs, a watchdog timeout triggers a hardware reset of the module. The DAC pin then returns to a high-impedance state, causing a brief transient in the output voltage; because the reset period is extremely short, this voltage fluctuation does not materially affect the module. Once the reset is completed, the system reinitializes the DAC and restores the default voltage output. Through the coordinated design of a hardware upper-voltage limit and a software-triggered reset, the system ensures that the output voltage never exceeds the module's safe operating voltage range under any fault condition.

4. System Software Design

The system software design flow is shown in Fig. 3.

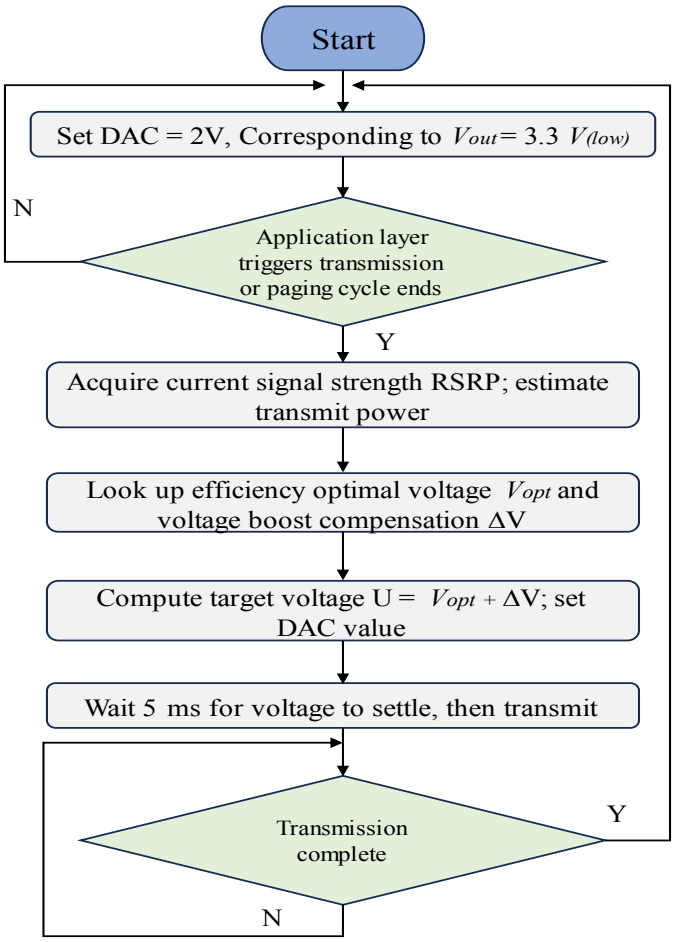

Fig. 3. System software design flow

The core objective of the software is to maximize the energy efficiency of each transmission while ensuring a stable communication link. When the device is in sleep or standby-monitoring mode, the system supplies power at the minimum voltage V_low (3.3 V), which is just sufficient to maintain the module's basic operation, minimizing static power consumption.

When the application layer has data pending for transmission, or the module receives a network scheduling command, the system first acquires the current signal strength (RSRP) and uses it to estimate the required transmit power; it then looks up the pre-configured efficiency-optimal voltage and voltage-boost compensation value. The signal-strength-based energy-efficiency optimization is shown in Table 1, whose data were obtained from laboratory characterization tests of the target module's power amplifier (PA).

Table 1. Signal-strength-based energy-efficiency optimization

Signal strength (dBm)	Transmit power (dBm)	Efficiency-optimal voltage (V)	Voltage-boost compensation (V)	Target voltage (V)
≥ −81	5	3.5	0.1	3.6
−96 to −81	13	3.7	0.15	3.85
−112 to −101	20	3.9	0.2	4.1
≤ −112	23	4.1	0.25	4.35

Each RSRP interval corresponds to a typical transmit-power level, together with the voltage value that gives the highest conversion efficiency and a safety compensation margin estimated from the peak current; summing the two yields the final target voltage. The software outputs the corresponding analog value via the DAC, which, through the op-amp adder, adjusts the BUCK power supply's feedback, driving the output voltage to settle at the target value precisely and quickly. This voltage satisfies the PA's highest-efficiency operating point at the current power level while retaining sufficient margin to offset the voltage drop that high current produces across path impedance, thereby preventing the cellular module from resetting owing to undervoltage. Once data transmission is complete, the voltage is rapidly restored to V_low.

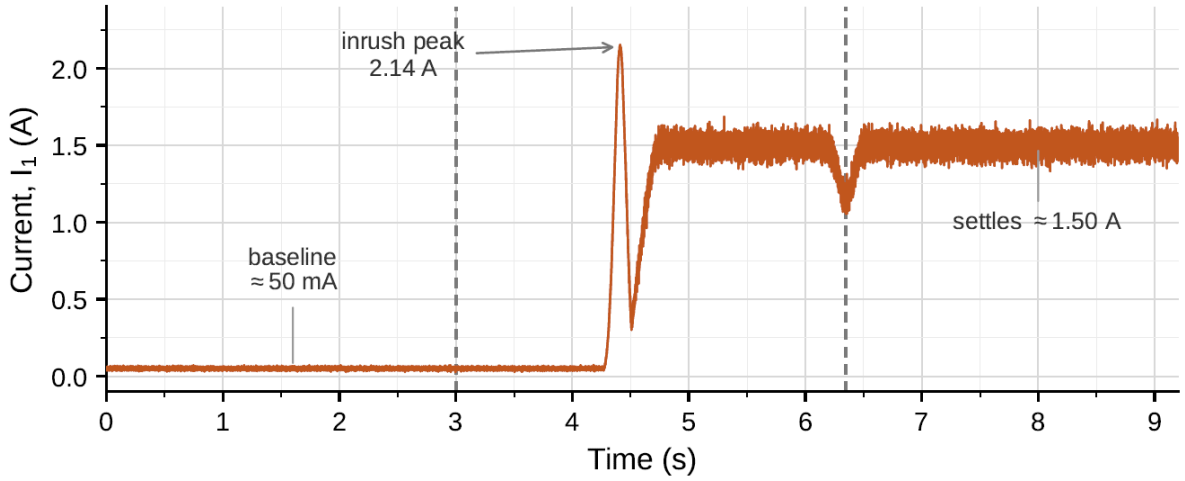

Fig. 4. Module transmit-current waveform

5. System Operation Results

To validate the performance of the reliable power supply system, tests were conducted on a test platform for the core operating scenario in which the cellular communication module switches instantaneously from standby to high-

power data transmission. The voltage and current waveforms on the supply line were captured simultaneously during testing.

The modules transmit-current waveform is shown in Fig. 4. When the system's operating state changes abruptly, the cellular module wakes from an idle state and executes a high-power data transmission: the load current surges from a standby value of 38.78 mA to a peak of 2.14 A. This characteristic pulsed-load behavior poses a severe challenge to the dynamic-response capability of the power supply system.

The dynamic-voltage-regulation output-voltage waveform is shown in Fig. 5, illustrating the effectiveness and benefits of the dynamic-regulation strategy. At the start of the test, the system outputs a lower voltage of 3.3 V, ensuring reduced power consumption while on standby. Before the high-current load arrives, the system software initiates the voltage-regulation routine, raising the output voltage to 3.8 V; when the peak current reaches 2.14 A, parasitic resistance in the power path causes a transient droop of approximately 0.3 V in the output voltage.

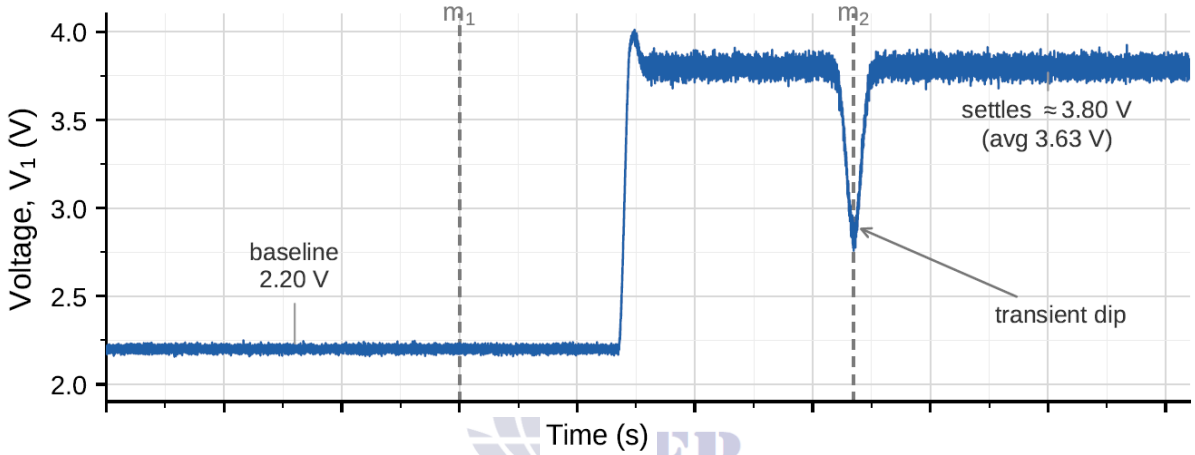

Fig. 5. Dynamic-voltage-regulation output-voltage waveform

These test results confirm the system's reliability: although a transient 0.3 V droop occurs, the pre-boost strategy ensures that the resulting minimum voltage remains above the module's reset threshold of 3.3 V, avoiding system restarts or communication interruptions caused by voltage droop. At the same time, the system does not operate in the high-voltage state at all times , during the great majority of low-power phases the voltage is maintained at approximately 3.3 V, which significantly reduces static power consumption, thereby optimizing energy efficiency while ensuring system reliability.

6. Conclusion

This paper proposes a software–hardware co-designed architecture that uses the cellular module as the core of power management: leveraging its built-in DAC and ADC resources, the system achieves precise closed-loop voltage control with minimal peripheral circuitry. The adopted efficiency-optimal pre-boost algorithm ensures both system reliability and fine-grained energy management.

The proposed design effectively improves the long-term operating reliability of terminal devices under battery power or weak power-source conditions; by dynamically regulating voltage, it extends device endurance, offering a novel, low-cost, and efficient path toward addressing the power-supply shortcomings of IoT terminals. Future work may incorporate additional parameters, such as ambient temperature and battery health state, into the voltage-regulation decision model, and explore deeper integration of this architecture with energy-harvesting technology to further extend its applicability to emerging scenarios such as passive, battery-free IoT.

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