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DEVELOPMENT OF FPGA-BASED FRACTIONAL-ORDER PID CONTROLLER MODULE FOR AUTONOMOUS ROBOTS USING FOR THE APPLICATION INDUSTRY 4.0

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Abstract

Fractional-order PID controller plays an important role in various industrial applications. The FOPID is the expansion of the conventional PID controller based on fractional calculus. PID controller regulates temperature, flow, pressure, speed, and other process variables in industrial control systems. Therefore, this research intends to design and implement the real-time FPGA-based FOPID controller, which is complex regarding memory issues and energy consumption. Thus, this research uses the hybridized technique of fixed- and floating-point approach using Matlab and Xilinx Vivado. The proposed design is realized on a Zynq-7000 FPGA board, and the performance is improved in terms of dynamic range, speed, unlimited use of resources, efficiency, and less energy consumption.

1. INTRODUCTION

Fractional-order PID controllers are universal control structures widely used in industrial automation in dynamic systems. They are usually implemented in hardware using analogue or digital components or computer-based software. The popularity of PID controllers based on FPGA using the fixed point approach for shortening the design time, low power consumption, and reducing the number of resources [1]. From the industry point of view, PID controllers are used for control purposes, and DC-DC power and buck-type converters are used based on FPGA [2], [3], [4]. For time-varying, non-linear, real-time demanding higher systems, an improved particle swarm optimization algorithm is adopted to optimize fractional PID controller parameters [5], [6]. FPGA-based adaptive neuro fuzzy inference system for controlling the full vehicle nonlinear active suspension and the evolutionary algorithm has been applied to modify the parameters of PID controllers [7]. DC motors are employed in all sorts of robotic applications (such as mobile robots and robot assembly lines), in ball and platforms, disk drives, flight simulators, robotic prostheses, and unmanned aerial vehicles, which are based on FPGA using the PID and FOPID controllers [8], [9], [10]. In [11], the proposed GL method was used to implement an FOPID controller based on FPGA. The implemented controller exerted a favourable response compared to its integer-order counterpart. PID controllers have drawn more attention in industry automation due to their ease and robustness [12], [13], [14]. Further, in the design of a motion profile to control the movement of robotics using the PID controller based on FPGA [15], BLDC motor [16]. In the medical field, cardiac pacemakers are used for patients who suffer from bradycardia, and pacemaker controllers are required to provide stability between heart rate and the desired pre-set profile of the pacemaker based on FPGA [17]. FPGA-Based FOPID plays a key role in the development of industries because widely used controllers in the industries using that controller FPGA based with performance would increase.

2. Literature Review

2.1. FPGA Implementation of Fractional-order Controllers

PID is a simple and widely used controller in industry for controlling various systems and real-time processes, including pressure, temperature, level, and flow. In each cycle, the PID controller calculates the next output value using the measured error between the set point and measured process variables. However, the PID controller performs poorly, especially for non-linear systems, and may lead to instability. Thus, the FOPID controller is achieved by fractional ordering the PID controller's integral and derivative actions. This will help in achieving better performance for non-linear and higher-order systems. Implementing the FOPID controller on an FPGA can offer several advantages and benefits in specific applications. For example, FOPID gives a higher degree of flexibility and precision while implementing this on the FPGA, which allows the fine-tuning and customization of the controller parameters and structure. FPGA implementation gives real-time processing and fast execution, responding rapidly while dealing with complex systems with reduced power consumption. Over the years, various researchers have proposed the implementation of FOPID controllers using several types of FPGAs. For instance, Lima et al. proposed an implementation of PID controllers using an FPGA Spartan 3 board for a transfer function model, where the controller parameters are achieved using an auto-tuning optimization algorithm [18]. The authors of [18] have only implemented the PID controllers using an FPGA. However, in advance, the researchers of [19] have implemented the PID and FOPID controllers while implementing them with a QFT-based controller for a buck type of DC-DC converter using the same FPGA. Tustin's approximation technique is used for the fixed-point approach to obtain a faster settling time, stability, and least overshoot performance. Further, in [20], the authors investigated the implementation of a discrete PID controller for a converter using an FPGA Cyclone board. The fixed-point approach improves transient response performance, speed, reliability, range, and precision. In addition, the research also used an adder and a multiplier in FPGA to obtain the desired results. For another type of application, the authors of [21] have developed an adaptive neuro-fuzzy inference system to control the full vehicle non-linear active suspension system. The approximate values of neuro-fuzzy's signum function are obtained while implementing on the FPGA Spartan board, which is used for the evolutionary algorithms obtaining better performance like more efficiency and robustness [22]. Caputo's fractional definition has been discussed in [4] and [11] for implementing the FOPID controller on an FPGA Altera board for a transfer function model and permanent magnet brushless direct current motor. The pole interlacing and the Tustin method obtained the approximate values and compared the system's performance with optimization algorithms. In [22], the PSO algorithm was used. In contrast, in [23], a dynamic PSO algorithm was used for better high-speed, reliable performance with the least control efforts.

The FOPI controller was also implemented on the FPGA board to control the DC motor's speed and permanent magnetic synchronous motors [24], [25]. Tustin, Oustaloup, and power series expansion are the approximation techniques used for the fixed- and linear-point approaches for better performance in overshoot, setting time, steady state error, dynamic response, and less adjustment time. In [26] and [27], the researchers proposed the FOPID controller to control the speed of the DC motor and induction motors. For the hardware implementation of the FOPID controller, various FPGA boards were used to achieve better performance (Refer to Table 2). The Tustin method was used as an approximation technique to improve the performance and optimize the system. A genetic algorithm is used for obtaining adequate performance in overshoot, steady state error, settling time, speed, and power consumption. The speed control of DC motors using fixed- and integer-point approaches effectively achieved better control action [26]. As presented in [28] and [29], the authors proposed a fractional-order integrator/differentiator based on the GL operator using binomial expansion, quadratic, and piece-wise linear approximation techniques for implementation on the FPGA Nexus 4 board. The fixed, linear, and quadratic window approaches improved accuracy, efficiency, speed, reduced memory dependence, and maximum absolute error. Rajagopal et al. developed an adaptive sliding mode controller, a genetically optimized PID controller for the fractional-order induction motor with an uncertain load [9]. This paper used the Caputo fractional order for the fractional definition while implementing the fixed-point approach on the FPGA Kintex 7 board to achieve better stability, efficiency, variations, and load torque performance. In [23], two degrees of freedom digital FOPID controllers were proposed to control the speed of the DC series motor while implemented on the FPGA Altera 4 board. In this case, the pole-zero interlacing method was used as an approximation technique and tuned using an improved dynamic PSO algorithm. Karthikeyan et al. developed a fractional-order adaptive sliding mode controller using a Caputo fractional-order while implementing the FPGA Kintex 7 board [30]. Binomial expan sion is used as an approximation technique for achieving better performances in power efficiency, speed, and the number of threads increased. The researchers of [31] have developed an FPGA-based low-cost robotic prosthesis with motor disabil ities in their upper limbs. The FOPID embedded controller was designed as an elbow joint-based DC motor in a robotic prosthesis implemented on the FPGA Artix 7 board. The tangent line, two-point method was used as an approximation technique for the approximate values of the FOPID controller, which were obtained using the Ziegler-Nicholas technique. The controller has achieved better performance in settling time, percentage overshoot and integral errors. A fixed-point approach is used in [32] to design a digital PID controller on the FPGA Spartan 6 board. The FPGA-based digital PID controller designed for high-speed DC motors delivered an optimal balance of insignificant risk, low cost, and low power. An approximated Tustin and Taylor series expansion-based FOPID controllers were proposed for brushless DC motors using Altera Cyclone III FPGA and a transfer function model using Sparton-6 FPGA in [16] and [33], respectively. The computational results for both systems have shown the robust ness, simple structure, flexible control, motor speed regulation, and versatility of the technology. Similarly, Tustin and direct torque control-based FOPID controllers using FPGA were designed to control the DC and induction motors' speed [34], [35]. For FPGA implementation, fixed and linear window approaches were used. The proposed drive system in [33] allows full load torque control with fast response and reduced torque ripple wide range for ripple variations. For a similar system, the FOPI controller-based direct torque control scheme was implemented using an FPGA Spartan 6 board and achieved improved efficiency and speed [36]. Further, in [37] and [38], an FPGA-based FOPID controller was developed to control the DC-DC converter and enhance switched reluctance motor performance. The modified PSO based FOPID controller implemented on Artix-7 Basys-3 and Sparton-6 FPGA uses Tustin, bi-linear, and torque ripple minimization techniques for achieving the desired performance. The FPGA-based FOPIDs have achieved extreme performance in increased output torque and faster settling time. An FPGA based robotic manipulator using dual PID controllers, optimized using the Chien-Hrones-Reswick technique, is proposed to reduce the overshoot and improve the system's energy conservation [15]. A fractional-order mersister circuit consisting of magnetic-controlled and charge-controlled implemented using GL technique on FPGA Cyclone 4 board for better performance in time response and less utilization of hardware resources with high accuracy [39]. An FPGA Artix 7 board has been used for the hardware implementation of an adaptive neuro-fuzzy inference system-based controller for a cardiac pacemaker for patients with bradycardia [40], [41]. The linear window approach achieves adequate performance like transient response, stability, steady state error, settling time, and power consumption. Artix 7 and Cyclone 5 FPGAs were used to implement the parameter-switching chaos control for the fractional-order spherical systems to encrypt the images [42]. Both FPGAs have obtained better performance in image encryption. Finally, the fractional and integer orders were used to develop an FPGA-based controller approximated using Tustin for temperature control in a Deusto heater [43]. A fixed-point approach is used for FPGA implementation and optimized using the modified Ziegler Nichols to obtain better load disturbance performance and maximum sensitivity.

Table 1. Summary of Works Focused on FPGA implementation of fractional order controllers.

Ref.	**Year**	**Controller**	**Approach**	**System**	**Approx. Method**	**FPGA Board**	**Tools/Simulator**	**Language**	**Slices**	**Freq.**	**Registers**
[18]	2006	PID	Floating & Fixed	Plant TF	-	Spartan-3 XC3S1000	MATLAB, ModelSim	C++, VHDL	3584	57.72 MHz	-
[19]	2008	PID, FOPID	Fixed-point	DC-DC Converter	Tustin	Spartan-3 DSP	Xilinx, MATLAB	-	628	125 kHz	628
[20]	2009	Discrete PID	Fixed-point	Converter	-	Cyclone EP1C6	Quartus, MATLAB	VHDL	1377	50 MHz	97
[21]	2010	ANFIS, FOPID	-	Nonlinear Suspension	Signum	Spartan XC3S700AN	MATLAB, Simulink	VHDL	-	-	-
[21]	2010	FOPID	-	Plant TF	-	Altera EP1C3T	MATLAB, ModelSim	HDL, VHDL	-	-	-
[24]	2013	FOPI	Floating & Fixed	DC Motor	Tustin	NI cRIO FPGA	LabVIEW, MATLAB	-	3441 / 3679	44.2 MHz	4236 / 3120
[26]	2013	FOPID	Double & Fixed	DC Motor	Tustin	Virtex-II / Spartan-3E	LabVIEW	-	14336 / 4656	55 – 70 MHz	28672 / 9312
[28]	2016	Frac. Integrator/Diff.	Window-based	-	Binomial	XC2V3000 FPGA	LabVIEW	VHDL	2852	20 Hz	2538

2.2. Fractional-order Definitions, PID Controllers and Approximations

The integration and derivatives are generalized by fractional calculus to non-integer order fundamental operators ${}_{a}D^{\mu}$, where a and t are operation's bounds and are real numbers [29]. The definition of continuous integer-differential operator is defined as,

$$a\,D_t^{\mu} = \begin{cases} \frac{d^{\mu}}{dt^{\mu}}, & \mu > 0, \\ 1, & \\ \int_a^t (dt)^{\mu}, \mu < 0. & \end{cases}$$

(1)

The most commonly used fractional definitions for the above fractional operator are the GL, the Riemann Liouville, and Caputo [28]. The GL fractional derivative operator for $\mu > 0$ and $t \in R$ is defined as,

$$D_t^{\mu} = \lim_{h->0} \sum_{j=0}^{\infty} (-1)^j \binom{\mu}{j} f(t - jh),$$

(2)

The binomial coefficients μ j can be computed as,

$\binom{\mu}{0} = 1, \binom{\mu}{j} = \frac{\Gamma(\mu+1)}{\Gamma(j+1)\Gamma(\mu-j+1)}, j = 1, 2, 3, \ldots$2) Fractional-order PID Controller: A PID controller with gain coefficients Kp, Ki and Kd utilizing a closed-loop feedback system to regulate all process variables is defined as [32].

$$C\,(s) = K_p + \frac{ki}{s} + K_d s.$$

(3)

From the above equation, the FOPID controller is obtained as follows [37].

$$C(s) = K_p + \frac{K_i}{s^{\alpha}} + K_d s^{\beta}, 0 < \alpha, \beta < 2,$$

(4)

Where α and β are the integrator and differentiator orders. 3) Fractional-order Approximations: There are numerous techniques for approximating fractional-order integrators and differentiators. Some of the most well-known approximation techniques include Oustaloup and Tustin, which are used for GL, Riemann-Liouville and Caputo fractional definitions. Tustin's approximation involves discretizing the continuous time FOPID controller into a discrete time to implement on the digital hardware. Tustin's approximation is one of the methods to discretize a continuous-time transfer function. The discretization c(z) of continuous-time transfer function c(s) is obtained as:

$$c(z) = c(s'), \text{where } s' = \frac{2}{T}\frac{z-1}{z+1}$$

(5)

In the Recursive Tustin method, the discretization is based on the approximation of s^{μ} the Tustin generating function, given as

$$s^{\mu} = \frac{2^{\mu}}{T}\left(\frac{1-z^{-1}}{1+z^{-1}}\right)\mu$$

(6)

3. Research Methodology

The flow chart for the respective activities for the proposed methodology towards achieving the research objectives is given below in Fig. 1. There are five phases in this research. They were explained as follows:

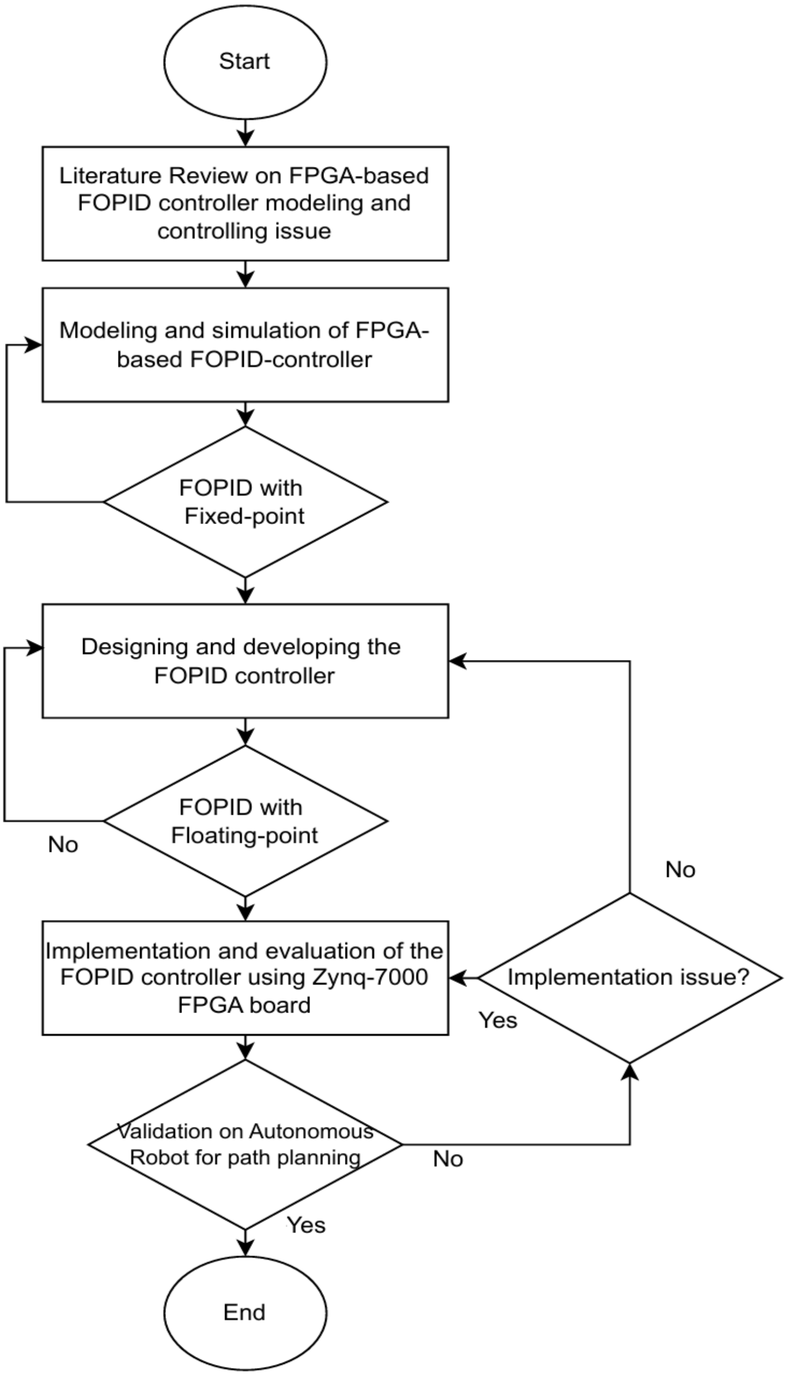


Fig 1. Research Methodology Flowchart

Phase 1: Preliminary Research
During this phase, the latest literature reviews on issues in FPGA implementation techniques and FOPID controllers are studied with practical publications.

Phase 2: To design FOPID controller using a hybrid fixed and floating-point approach in Matlab and Xilinx
In this phase, design a model of the FOPID controller in MATLAB Simulink for first defining the fractional order transfer function in the form of the equation. Then, convert that fractional order transfer function into the discrete-time representation applicable for HDL

language in Matlab. After that, the hybrid technique is applied to the model, and the fixed-point approach is used for the energy consumption. After that, we use the floating point for the accuracy and efficiency of the model refer to Fig. 2, after simulating the system and checking the performance and response of the system. Then, generate the HDL code into the model and validate that code in Simulink with the system's performance. In the last, convert that HDL code into VHDL code to generate a bit-stream into the FPGA.

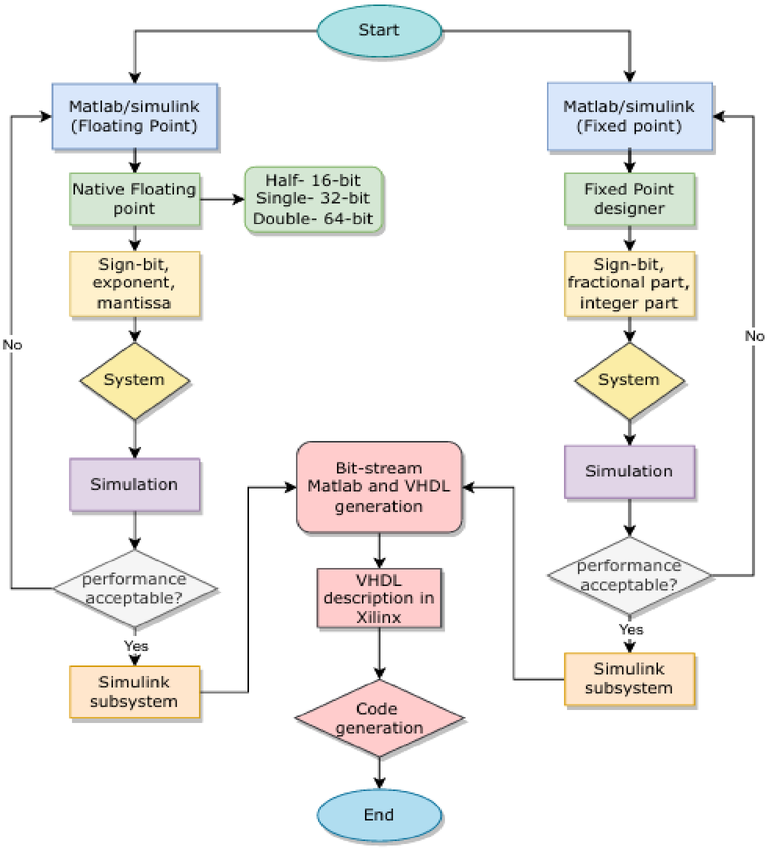


Fig 2. Fixed- and Floating-point Hybrid model

Phase 3: To develop FPGA-based FOPID controller in Zynq 7000 FPGA board

During this phase, the simulation of the FPGA-based FOPID controller, after the selection of the board through the Xilinx boards directory, generates the code into the Zynq-7000 FPGA board and connects with Xilinx Vivado. During literature re views (Refer to table no: II), researchers use many boards, and Zynq-7000 is our choice to implement the FOPID controller on it. The Zynq-7000 combines an FPGA fabric ARM cortex A9 processor with the environment FPGA and ARM cores, 20 times greater processing performance than a single Micro Blaze core. The energy consumption range of the Zynq-7000 is less than the other FPGAs (1.2V to 3.3V). Zynq-7000 board is given below in Fig. 3 with labelling.

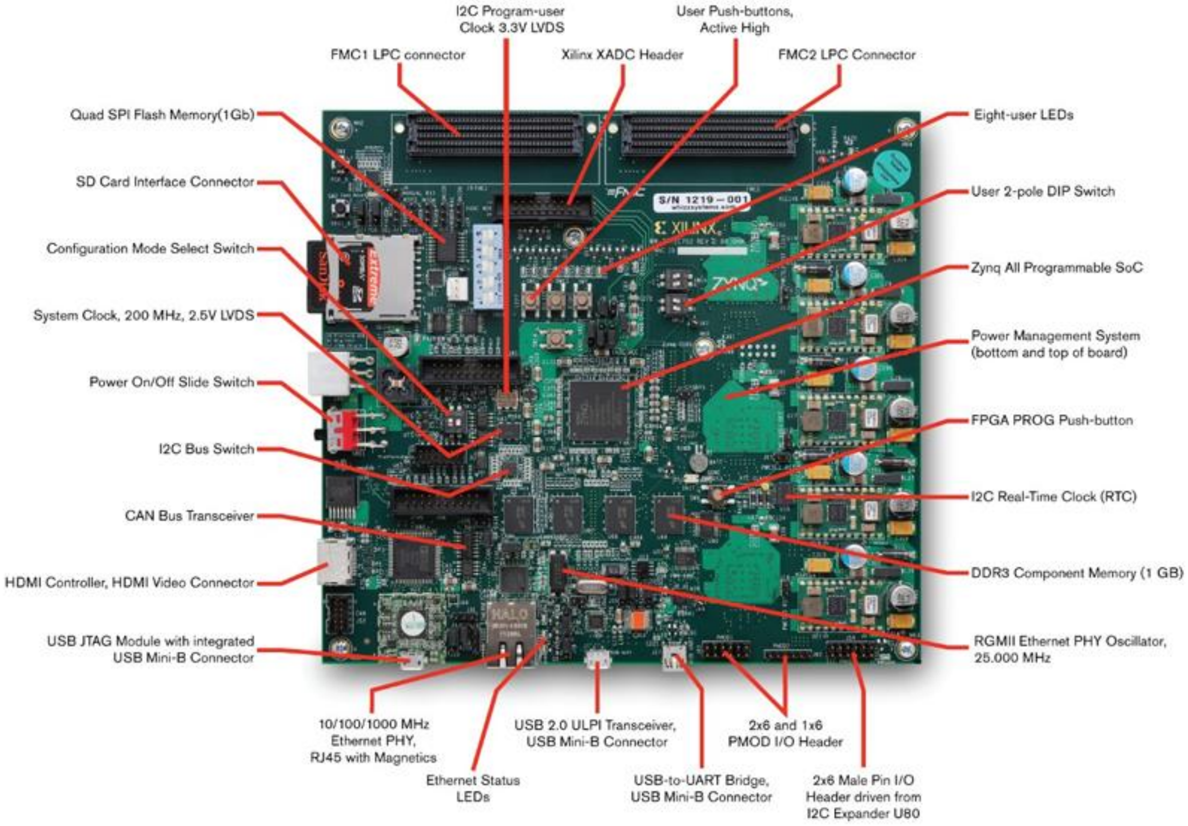


Fig 3. Zynq-7000 FPGA board

Phase 4: To implement and evaluate the FPGA-based FOPID controller for autonomous mobile robots for path planning and obstacle avoidance

The main object of this phase is to implement the FPGA based FOPID controller for autonomous mobile robots with hybrid approaching points. Previously, FOPID controllers were implemented using FPGA, but dynamic range, accuracy, efficiency, and energy consumption are not up to mark. That's why the hybrid model is used on an FPGA-based FOPID controller, which will give us better performance in terms of efficiency, accuracy, dynamic range, energy consumption, and utilization of the resources in the unlimited and the autonomous robot will perform tasks like navigation, so FOPID controller integrates with the navigation algorithm to make high-level decisions and control robot's motion. The FPGA-based controller will provide precise control and adaptability to different robot's behaviours and environments.

Phase 5: Testing and validation.

During this phase, the FOPID controller will be tested and validated on the FPGA using hybrid fixed-and floating point for the autonomous mobile robots, and performance will be evaluated in terms of resource utilization, dynamic range, efficiency, accuracy, and in the form of energy consumption.

4. Result and Discussion

4.1. Modelling of PID controller

In this, Matlab is used to simulate the discrete PID controller using the simple transfer function. In this, the response of the PID controller is in stable condition without applying the tuning method. The equation of the PID controller is given below, and the model of the PID controller is referred to in Fig. 4

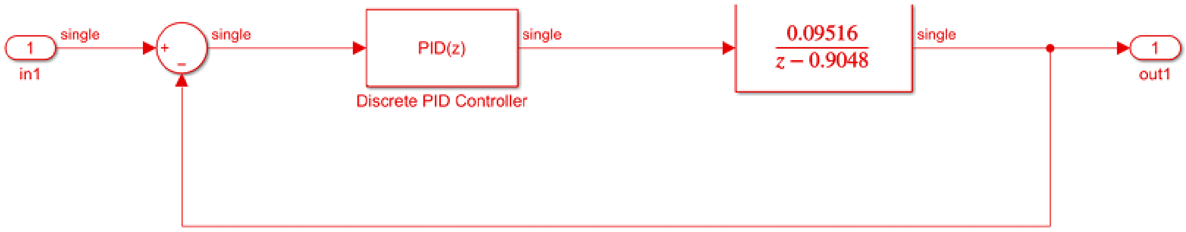


Fig 4. PID controller.

The response of the Discrete PID controller with the transfer function is stable, now applying the automatic tuning method on the PID controller, so the performance of the PID controller plays an important role in the desired control refer to Fig. 5 and Fig. 6.

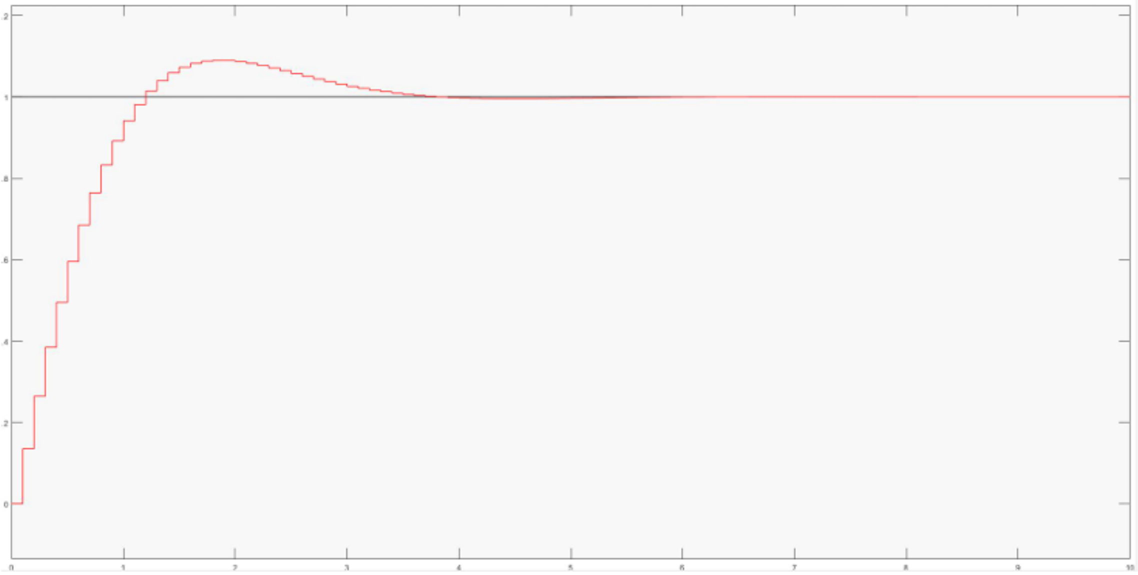


Fig. 5. Response of Discrete PID controller

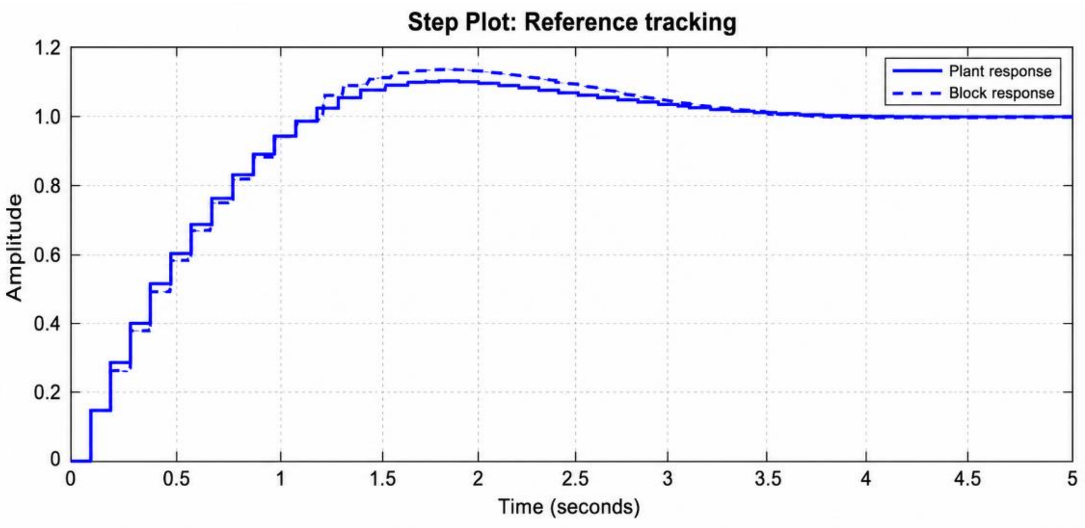


Fig. 6. Response of tuned Discrete PID-controller

4.2. HDL code generation

In Fig. 7, the model of the Discrete PID controller with transfer function is used to check the controller's response. Now, change them into a subsystem to apply the HDL code generation with constant signal and apply the floating-point approach on the controller for desired performance like unlimited use of resources. Then, check that model in Model Advisor using Matlab. The fixed-point approach is also applied in that model for less energy consumption and accuracy. Set the target of the FPGA Zynq-7000 board refer to Fig. 3 using Matlab, then generate the HDL code into the controller Refer to Fig. 7, and after the generation of code, validate and test the model in Matlab.

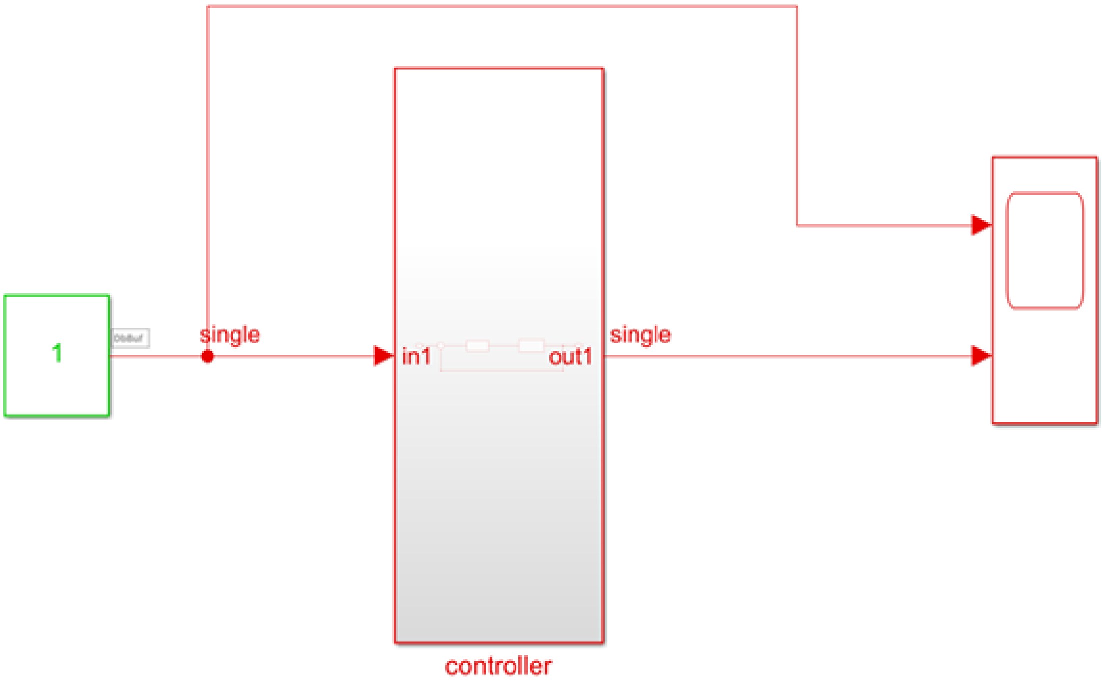


Fig 7. Controller (subsystem)

4.3. HDL into VHDL

The code is generated into the model in HDL language, and Matlab converts that code into VHDL for Xilinx to check the results, synthesized design of the FPGA-based discrete PID controller in Fig. 8 and the power utilization report of FPGA is given in Fig. 9.

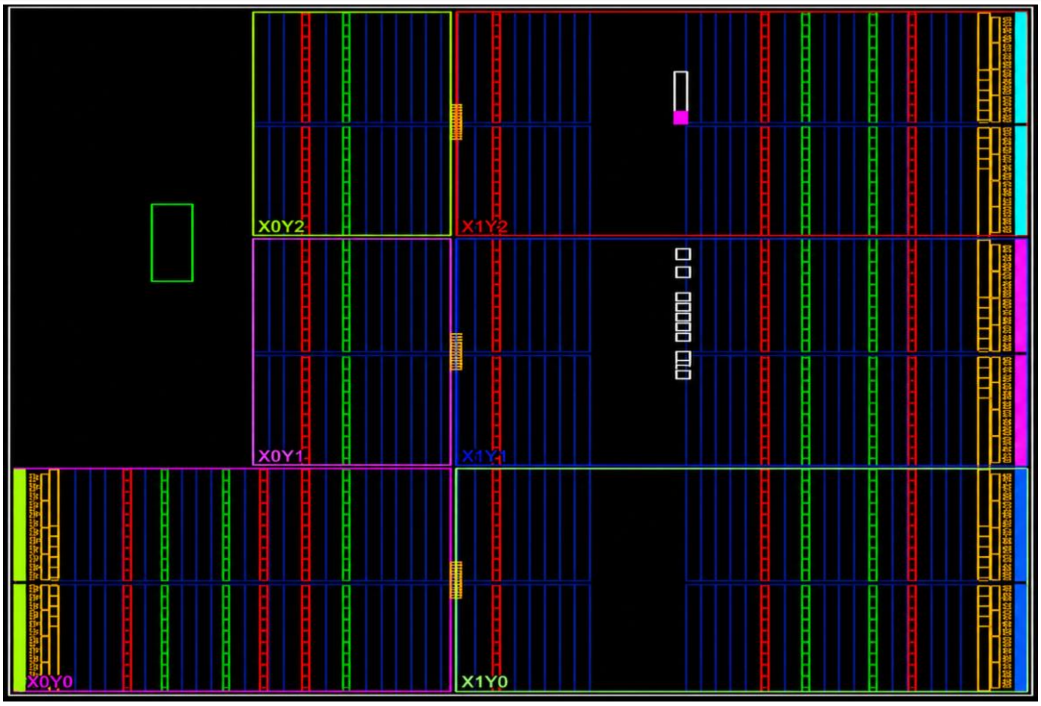
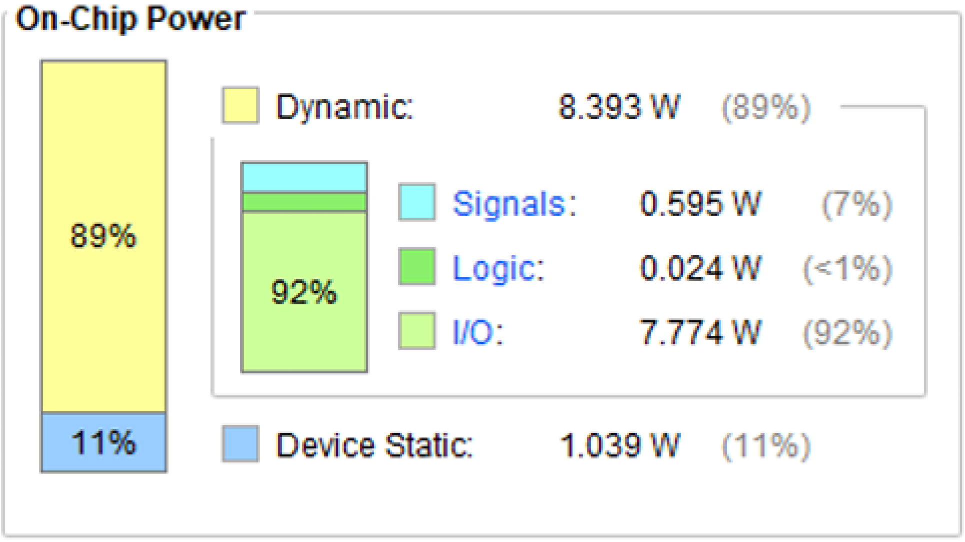


Fig. 8. Synthesized design of Discrete PID controller



On-Chip Power

	Dynamic:	8.393 W	(89%)
	Signals:	0.595 W	(7%)
	Logic:	0.024 W	(<1%)
	I/O:	7.774 W	(92%)
	Device Static:	1.039 W	(11%)

Fig 9. Power consumption report

5. Conclusion

A PID controller model has been developed using the hybrid fixed-and floating-point approaches implemented on the FPGA. PID controller is used with a simple transfer function to validate the model with hybrid approaches. Finally, the performance of this model seems to be better in terms of dynamic range, accuracy, unlimited use of resources, speed, and energy consumption of the model.

ABBREVIATIONS

FOPI	Fractional-order PI
FOPID	Fractional-order PID
FPGA	Field-programmable Gate array
GL	Gru¨nwald Letnikov
HDL	Hardware Description Language
LUT	Look Up Table
HDL	High Definition Language
UHDL	Very High-Speed Integrated Circuit Hardware Description Language

MCU	Microcontroller unit
PID	Proportional Integral and Derivative
PSO	Particle Swarm Optimization
QFT	Quantitative Feedback Theory
SRAM	Static Random-access Memory
Xilinx IDE	Xilinx Integrated Design Environment
Xilinx ISE	Xilinx Integrated Software Environment

REFERENCES

Y. F. Chan, M. Moallem, and W. Wang, “Design and implementation of modular FPGA-based PID controllers,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1898–1906, 2007, doi: 10.1109/TIE.2007.898283.

E. William, J. Linares-Flores, E. Guzman-Ramirez, and H. Sira-Ramirez, “FPGA Implementation of PID Controller for the Stabilization of a DC-DC ‘Buck’ Converter,” *Front. Adv. Control Syst.*, 2012, doi: 10.5772/39083.

L. Lv, C. Chang, Z. Zhou, and Y. Yuan, “An FPGA-based modified adaptive PID controller for DC/DC buck converters,” *J. Power Electron.*, vol. 15, no. 2, pp. 346–355, 2015, doi: 10.6113/JPE.2015.15.2.346.

M. C. Rozina Chohan, Imran Mir Chohan, “Comparative Analysis of Different Convergent Dection Angles and Working Fluids on Supersonic Nozzle Thrust Force by Computational Fluid Dynamic (CFD),” *Tech. J.*, vol. Vol 30, no. 02, 2025.

R. Shahouni, M. Bahraini, M. Abrofarakh, and M. Abbasi, “Adaptive tuning of fractional order PID controllers for nonlinear processes using hybrid PSO DQN reinforcement learning,” *Sci. Rep.*, vol. 15, no. 1, 2025, doi: 10.1038/s41598-025-22509-x.

I. Mir Chohan *et al.*, “Corrosion Behaviour and Microhardness of ASTM 106 Grade B Carbon Steel Offshore Pipeline at Different Locations in Malaysia,” *J. Adv. Res. Micro Nano Eng. J. homepage*, vol. 38, pp. 1–11, 2025, [Online]. Available: https://semarakilmu.com.my/journals/index.php/micro_nano_engineering/index

K. Lapa and K. Cpalka, “Flexible Fuzzy PID Controller (FFPIDC) and a Nature-Inspired Method for Its Construction,” *IEEE Trans. Ind. Informatics*, vol. 14, no. 3, pp. 1078–1088, 2018, doi: 10.1109/TII.2017.2771953.

P. S. Panwar, M. Gupta, S. Mondal, and A. Kumar, “PID embedded control and DC motor behavior for FPGA-based simulation,” *Embed. Devices Internet Things Technol. Appl.*, pp. 63–85, 2024, doi: 10.1201/9781003510420-4.

E. Minca, A. Filipescu, and A. Voda, “Modelling and control of an assembly/disassembly mechatronics line served by mobile robot with manipulator,” *Control Eng. Pract.*, vol. 31, pp. 50–62, 2014, doi: 10.1016/j.conengprac.2014.06.005.

S. Kumar, H. Sakidin, M. Zafar, H. B. Lanjwani, and I. M. Chohan, “Nanofluid Thermophysical Property Modeling for Enhanced Oil Recovery: A Comprehensive Review and Future Outlook for Artificial Intelligence Integration,” *Arch. Comput. Methods Eng.*, 2025, doi: 10.1007/s11831-025-10329-1.

M. F. Tolba, L. A. Said, A. H. Madian, and A. G. Radwan, “FPGA Implementation of the Fractional Order Integrator/Differentiator: Two Approaches and Applications,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2019, pp. 1484–1495. doi: 10.1109/TCSI.2018.2885013.

S. Skoczowski, S. Domek, K. Pietrusewicz, and B. Broel-Plater, “A method for improving the robustness of PID control,” *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1669–1676, 2005, doi: 10.1109/TIE.2005.858705.

V. M. Alfaro and R. Vilanova, “PID control: Resilience with respect to controller implementation,” *Front. Control Eng.*, vol. 3, 2022, doi: 10.3389/fcteg.2022.1061830.

I. M. Chohan, A. Ahmad, N. Bheel, T. Najeh, and A. H. Almaliki, “Sustainability assessment of different pipeline materials in freshwater supply systems,” *Front. Mater.*, vol. 12, 2025, doi: 10.3389/fmats.2025.1566151.

P. Chotikunnan and R. Chotikunnan, “Dual Design PID Controller for Robotic Manipulator Application,” *J. Robot. Control*, vol. 4, no. 1, pp. 23–34, 2023, doi: 10.18196/jrc.v4i1.16990.

F. Zhang and Z. Li, “Design of fractional PID control system for BLDC motor based on FPGA,” in *Proceedings of the 30th Chinese Control and Decision Conference, CCDC 2018*, 2018, pp. 2293–2296. doi: 10.1109/CCDC.2018.8407508.

M. E. Crowe, C. T. Hayes, and Z. U. Hassan, “Using software-based simulation for resident physician training in the management of temporary pacemakers,” *Simul. Healthc.*, vol. 8, no. 2, pp. 109–113, 2013, doi: 10.1097/SIH.0b013e31826ec3e1.

J. Lima, R. Menotti, J. M. P. Cardoso, and E. Marques, “A methodology to design FPGA-based PID controllers,” *Conf. Proc. - IEEE Int. Conf. Syst. Man Cybern.*, vol. 3, pp. 2577–2583, 2006, doi: 10.1109/ICSMC.2006.385252.

B. Jayakrishna and V. Agarwal, “FPGA implementation of QFT based controller for a buck type DC-DC power converter and comparison with fractional and integral order PID controllers,” in *11th IEEE Workshop on Control and Modeling for Power Electronics, COMPEL 2008*, 2008. doi: 10.1109/COMPEL.2008.4634689.

Y. Xu, K. Shuang, S. Jiang, and X. Wu, “FPGA implementation of a best-precision fixed-point digital PID controller,” *2009 Int. Conf. Meas. Technol. Mechatronics Autom. ICMTMA 2009*, vol. 3, pp. 384–387, 2009, doi: 10.1109/ICMTMA.2009.517.

A. A. Aldair and W. Wang, “FPGA Based Adaptive Neuro Fuzzy Inference Controller for Full Vehicle Nonlinear Active Suspension Systems,” *Int. J. Artif. Intell. Appl.*, vol. 1, no. 4, pp. 1–15, 2010, doi: 10.5121/ijaia.2010.1401.

L. Qu, H. Hu, and Y. Huang, “Fractional order PID controller based on particle swarm optimization implemented with FPGA,” in *Proceedings - International Conference on Artificial Intelligence and Computational Intelligence, AICI 2010*, 2010, pp. 165–169. doi: 10.1109/AICI.2010.41.

S. Khubalkar, A. Junghare, M. Aware, and S. Das, “Modeling and control of a permanent-magnet brushless DC motor drive using a fractional order proportional-integral-derivative controller,” *Turkish J. Electr. Eng. Comput. Sci.*, vol. 25, no. 5, pp. 4223–4241, 2017, doi: 10.3906/elk-1612-277.

C. I. Muresan, S. Folea, G. Mois, and E. H. Dulf, “Development and implementation of an FPGA based fractional order controller for a DC motor,” *Mechatronics*, vol. 23, no. 7, pp. 798–804, 2013, doi: 10.1016/j.mechatronics.2013.04.001.

Afsheen, Mujtaba Hassan, Imran Mir Chohan, Sadaquat Hussain, and Raja Zafar Ali, “Supply Chain Management Impact on Project Performance in Construction,” *Spectr. Eng. Sci.*, vol. 3, no. 8, 2025, [Online]. Available: https://doi.org/10.5281/zenodo.16886237

C. I. Muresan, G. Mois, S. Folea, and C. Ionescu, “Alternative implementations of a fractional order control algorithm on FPGAs,” *2013 Int. Conf. Reconfigurable Comput. FPGAs, ReConFig 2013*, 2013, doi: 10.1109/ReConFig.2013.6732269.

A. Karthikeyan and K. Rajagopal, “Chaos control in fractional order smart grid with adaptive sliding mode control and genetically optimized pid control and its FPGA implementation,” *Complexity*, vol. 2017, 2017, doi: 10.1155/2017/3815146.

K. P. S. Rana, V. Kumar, N. Mittra, and N. Pramanik, “Implementation of fractional order integrator/differentiator on field programmable gate array,” *Alexandria Eng. J.*, vol. 55, no. 2, pp. 1765–1773, 2016, doi: 10.1016/j.aej.2016.03.030.

M. F. Tolba, L. A. Said, A. H. Madian, and A. G. Radwan, “FPGA Implementation of the Fractional Order Integrator/Differentiator: Two Approaches and Applications,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 66, no. 4, pp. 1484–1495, 2019, doi: 10.1109/TCSI.2018.2885013.

K. Rajagopal, F. Nazarimehr, A. Karthikeyan, A. Srinivasan, and S. Jafari, “Fractional Order Synchronous Reluctance Motor: Analysis, Chaos Control and FPGA Implementation,” *Asian J. Control*, vol. 20, no. 5, pp. 1979–1993, 2018, doi: 10.1002/asjc.1690.

IEEE Instrumentation and Measurement Society, Annual IEEE Computer Conference, IEEE International Symposium on Medical Measurements and Applications 9 2014.06.11-12 Lisbon, and MeMeA 9 2014.06.11-12 Lisbon, “IEEE MeMeA 2014 - IEEE International Symposium on Medical Measurements and Applications, Proceedings,” *IEEE MeMeA 2014 - IEEE Int. Symp. Med. Meas. Appl. Proc.*, 2014.

K. Lee and Y. Kim, “Design and Analysis of Digital PID Controller in MCU and FPGA,” in *Proceedings - International SoC Design Conference 2018, ISOCC 2018*, 2018, pp. 261–262. doi: 10.1109/ISOCC.2018.8649909.

O. Chandra Sekhar and S. Lakhimsetty, “Direct torque control scheme for a five-level multipoint clamped inverter fed induction motor drive using fractional-order PI controller,” *Int. Trans. Electr. Energy Syst.*, vol. 30, no. 9, 2020, doi: 10.1002/2050-7038.12474.

D. Fister, A. Jakopič, and M. Truntič, “Control Applications with FPGA: Case of Approaching FPGAs for Students in an Intelligent Control Class,” *Appl. Sci.*, vol. 15, no. 24, 2025, doi: 10.3390/app152412884.

I. M. Chohan, A. Ahmad, N. Sallih, N. Bheel, W. M. Salilew, and A. H. Almaliki, “Effect of seawater salinity, pH, and temperature on external corrosion behavior and microhardness of offshore oil and gas pipeline: RSM modelling and optimization,” *Sci. Rep.*, vol. 14, no. 1, 2024, doi: 10.1038/s41598-024-67463-2.

O. Chandra Sekhar, S. Lakhimsetty, and A. H. Bhat, “A comparative experimental analysis of fractional order PI controller based direct torque control scheme for induction motor drive,” *Int. Trans. Electr. Energy Syst.*, vol. 31, no. 1, 2021, doi: 10.1002/2050-7038.12705.

S. Negi, Y. S. Kushwaha, P. Dwivedi, and S. Bose, “Design and Performance Analysis of FPGA based Fractional-PID Controller,” *2021 Asian Conf. Innov. Technol. ASIANCON 2021*, 2021, doi: 10.1109/ASIANCON51346.2021.9545075.

A. Manjula, L. Kalaivani, and M. Gengaraj, “Pso based torque ripple minimization of switched reluctance motor using fpga controller,” *Intell. Autom. Soft Comput.*, vol. 29, no. 2, pp. 451–465, 2021, doi: 10.32604/iasc.2021.016088.

Z. Szadkowski, “Front-end board with cyclone V as a test high-resolution platform for the auger-beyond-2015 front end electronics,” in *IEEE Transactions on Nuclear Science*, 2015, pp. 985–992. doi: 10.1109/TNS.2015.2426059.

I. M. Chohan, A. Ahmad, N. Sallih, N. Bheel, and A. H. Almaliki, “Effect of seawater salinity and temperature on material performance and marine ecotoxicity of offshore pipeline using RSM modelling,” *Int. J. Environ. Sci. Technol.*, vol. 23, no. 2, 2026, doi: 10.1007/s13762-025-06869-5.

I. M. Chohan, A. Ahmad, N. Sallih, N. Bheel, and A. Almaliki, “Correction: Effect of seawater salinity and temperature on material performance and marine ecotoxicity of offshore pipeline using RSM modelling,” *Int. J. Environ. Sci. Technol.*, vol. 23, no. 3, 2026, doi: 10.1007/s13762-025-07011-1.

H. Homulle and E. Charbon, “Performance characterization of Altera and Xilinx 28 nm FPGAS at cryogenic temperatures,” *2017 Int. Conf. Field-Programmable Technol. ICFPT 2017*, vol. 2018-January, pp. 25–31, 2017, doi: 10.1109/FPT.2017.8280117.

J. J. Gude and P. García Bringas, “Proposal of a Control Hardware Architecture for Implementation of Fractional-Order Controllers,” *Springer Proc. Math. Stat.*, vol. 454, pp. 229–262, 2024, doi: 10.1007/978-3-031-56496-3_16.