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DESIGN AND ANALYSIS OF LOW-LEAKAGE SRAM CELL IN SUB-30 NM CMOS TECHNOLOGY A COMPREHENSIVE REVIEW

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Abstract
As CMOS devices are moving into a range of less than 30 nm, leakage power has become a major issue for static random-access memory (SRAM) design. The SRAM blocks consume a significant area of modern system-on-chip designs, which are always active even during idle mode. This makes them more prone to leakage currents. This review paper aims to provide a detailed discussion on leakage issues for sub-30 nm CMOS devices, a thorough review of various low leakage techniques for designing static random-access memory, static noise margin, data retention voltage, read/write margins, process variations, supply voltage scaling, and temperature variations. In addition, a practical approach to designing a low leakage SRAM cell using conventional techniques is also explored. The aim is to provide a clear review of previously published research on low leakage techniques for designing static random-access memory while making connections between theoretical principles and practical considerations used during modern static random access memory design [1], [8].

I. INTRODUCTION

Static Random Access Memory is a basic element of modern digital systems, ranging from microprocessors to mobile devices and low-power embedded systems. With aggressive scaling of CMOS devices to sub-30nm nodes, memory density has been increased considerably, which allows designers to integrate large memory arrays on a chip. However, aggressive scaling has also posed serious challenges to power dissipation. Unlike DRAM memory, which has to be refreshed periodically, static memory cells consume constant power to retain data. Thus, leakage currents become a major issue that determines the power consumption of modern Nano-scale SRAM memory [1].

These challenges in sub-30 nm CMOS technologies are further compounded by the need for aggressive voltage scaling, threshold voltage reduction, and the presence of short channel effects. The traditional 6T SRAM cells designed for older technology nodes may fail to provide the required stability and data retention characteristics in these newer technologies. These challenges have led researchers to explore various low leakage SRAM architectures and circuit

styles that can effectively reduce standby power while ensuring read and write stability [2], [8].

Further, for newer applications such as portable electronics, Iota devices, and biomedical implants, the need for ultra-low-power operation has become increasingly important. In these applications, any leakage current can have a significant impact on the battery life of the device and hence needs careful consideration. Leakage currents and the need for its control have become increasingly important in the design of SRAM cells in recent years [1], [3].

2. Leakage Mechanisms in Scaled CMOS

Leakage mechanisms in scaled CMOS refer to the unwanted currents that flow in a transistor even when it is in the OFF state [8], [11], and these currents become more significant as CMOS technology scales to nanometer dimensions [4]. As device dimensions, threshold voltage, and oxide thickness are reduced to achieve higher speed and density, the control of the gate over the channel weakens, leading to increased leakage power [5], [8]. The major leakage mechanisms include subthreshold leakage, which occurs due to carrier diffusion when the gate-to-source voltage is below the threshold voltage [2], [6]; gate oxide tunneling leakage, caused by electrons tunneling through the extremely thin gate oxide [5], [8]; junction leakage, which flows through reverse-biased source–body and drain–body junctions [1], [8]; and gate-induced drain leakage (GIDL), which appears due to high electric fields near the drain region [8], [14]. These leakage currents significantly increase static power consumption, degrade energy efficiency, and pose serious challenges in low-power and memory-intensive circuits such as SRAM in deeply scaled CMOS technologies [10], [15], [16].

2.1 Sub threshold Leakage

Sub threshold leakage is the current that flows between the drain and source of a MOSFET even when the gate-to-source voltage is lower than the threshold voltage, meaning the transistor is ideally in the OFF state. In scaled CMOS technologies, the threshold voltage is reduced to maintain high performance at lower supply voltages, which weakens the gate's control over the channel and allows carriers to diffuse from source to drain. This leakage current increases exponentially with a decrease in threshold voltage and an increase in temperature, making it the dominant component of static power consumption in deep-submicron and nanometer-scale devices. Sub threshold leakage is especially critical in memory circuits such as SRAM, where a large number of transistors remain idle for long periods, leading to significant standby power dissipation and reduced energy efficiency [2], [6]. Sub threshold Leakage as shown in fig. 1.

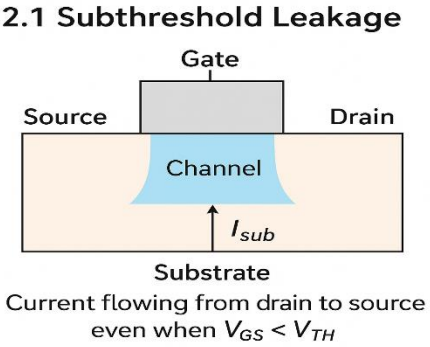

Fig.1 Sub threshold Leakage

2.2 Gate Oxide Tunneling

Gate oxide tunneling is a leakage mechanism that occurs due to electron tunneling through the ultra-thin gate oxide layer in scaled CMOS technologies. As device dimensions are reduced, the thickness of the gate oxide becomes extremely small (typically less than 2 nm), allowing charge carriers to quantum-mechanically tunnel through the oxide even when the transistor is in the OFF state. This results in leakage current flowing between the gate and the channel, source, or drain. Gate oxide tunneling significantly increases static power dissipation and

can also affect device reliability due to oxide degradation. To reduce this leakage, modern CMOS technologies employ high-k dielectric materials along with metal gates, which allow a physically thicker oxide while maintaining strong gate control over the channel [5], [8]. Where Electron tunneling through ultra-thin gate oxide as shown in fig. 2.

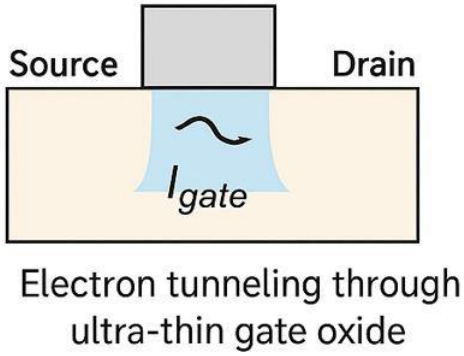

Fig.2 Electron tunneling through ultra-thin gate oxide

2.3 Junction Leakage

Junction leakage is the leakage current that flows across the reverse-biased p–n junctions formed between the source–body and drain–body regions of a MOS transistor. In scaled CMOS technologies, heavy doping concentrations and reduced junction dimensions increase the electric field within these junctions, leading to higher leakage currents. Junction leakage mainly occurs due to minority carrier diffusion and generation–recombination of carriers in the depletion region of the reverse-biased junction. This leakage current increases with temperature and contributes to the overall static power dissipation of the circuit. Although junction leakage is generally smaller compared to sub threshold leakage in advanced technologies, it still plays an important role in low-power and high-density designs such as SRAM and other memory circuits [1], [8]. The leavkage across revere'biases as shown in fig. 3.

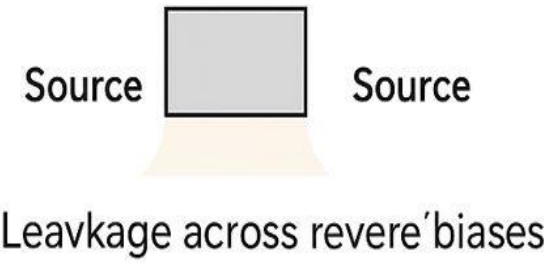

Fig. 3: Leavkage across revere'biases

2.4 Impact of Process Variation

Process variation refers to the unavoidable fluctuations in manufacturing parameters that occur during CMOS fabrication, such as variations in channel length, oxide thickness, doping concentration, and threshold voltage [4], [11]. In scaled CMOS technologies, these variations become more pronounced due to extremely small device dimensions and tight design margins [4], [10]. Process variations can significantly affect leakage currents by altering the threshold voltage and electric fields within transistors, leading to large device-to-device differences in subthreshold leakage, gate oxide tunneling, and junction leakage [8], [11], [14]. As a result, some transistors may exhibit much higher leakage than expected, increasing overall static power consumption and reducing yield and reliability [10], [15]. In memory circuits such as SRAMs, variations

can also affect the stability of the circuit and result in read and write failures, making variation-aware design techniques critical in deep scaling CMOS technologies [1], [2], [20]. The impact process variation as shown in fig. 4.

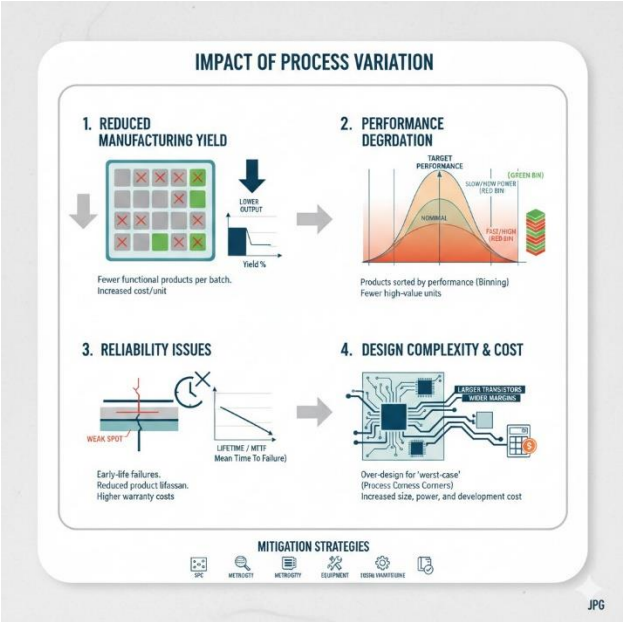

Fig. 4: Impact of Process Variation

3. Design Constraints for Sub-30 nm SRAM

Designing an SRAM cell in sub-30 nm technology nodes necessitates an appropriate balance of several critical constraints due to aggressive scaling effects on the device [1], [3], [6]. The stability of an SRAM cell is a key constraint and is often tested by measuring the Static Noise Margin (SNM), which reflects the capability of an SRAM cell to maintain its stored data in the presence of noise; a low Static Noise Margin poses a high risk of read and write failures [3], [7]. Retention is another key constraint and is characterized by the Data Retention Voltage (DRV), which reflects the minimum voltage at which an SRAM cell can retain its data without flipping; a very low DRV is crucial to ultra-low-power operations [6], [9].

In addition, the read and write performance should be ensured by providing sufficient read and write margins, despite the fact that the majority of the techniques for reducing leakage current often compromise the drive strength of the transistors and the access speed [1], [2]. Finally, the role of area and density is crucial since the main aim is to achieve the smallest cell area possible, despite the fact that techniques like transistor stacking may compromise the area [5], [10]. In conclusion, an efficient SRAM design for sub-30 nm technology requires an efficient trade-off between stability, retention, performance, and area to achieve the required power consumption without compromising the reliability of the SRAM cell [1], [6], [10].

4. Review of Low-Leakage SRAM Design Techniques

As CMOS devices continue to shrink into sub-30 nm geometries, leakage power is a major issue to be considered during SRAM design because of the decrease in threshold voltage. In order to overcome leakage power issues, several low leakage power techniques have been proposed and implemented during SRAM design [14, 15, 16]. One technique is multi-threshold CMOS, which involves using high threshold voltage transistors for non-critical paths to reduce leakage power. Another technique is transistor stacking, which is used to decrease leakage power by increasing the threshold voltage when several OFF transistors are stacked [17, 18]. Power gating and sleep transistor techniques are also used

to switch off the supply voltage to idle memory blocks to decrease leakage power [14].

In addition, assist techniques such as read-assist and write-assist circuits are useful in ensuring stability and performance while operating at low voltage supplies [1], [2]. The usage of high-k/metal gate materials reduces gate oxide tunneling leakage [5], [8]. These techniques allow for the development of low leakage power and stable and reliable SRAM cells while maintaining performance in deep-scaled CMOS [15], [16], [17].

4.1 Multi-Threshold CMOS (MTCMOS)

A widely used technique for reducing leakage current in SRAM circuits is called MTCMOS and is used by employing transistors with different threshold voltages to optimize power and performance in SRAM circuits [5], [6], [14]. In MTCMOS, high-VTH transistors are used in non-critical path and standby regions to minimize the sub-threshold leakage current in SRAM circuits, while low-VTH transistors are used in critical path regions to ensure high-speed operation and good read and write performance [5], [6], [14]. During normal operation, SRAM circuit operation is normal with minimal performance degradation, and when the SRAM circuit is in standby mode, leakage current is minimized using high-VTH transistors or sleep transistors [14], [19]. Although MTCMOS is an effective technique for reducing static power in SRAM circuits operating in sub-30nm technology nodes, it also poses some issues related to process complexity and sizing to avoid degradation in circuit stability and access time [5], [6], [17].

4.2 Transistor Stacking

One of the most common techniques used in the design of CMOS digital circuits is transistor stacking, which is effective in reducing leakage current, especially in scaled CMOS technology. In transistor stacking, a group of transistors is connected in series between the power supply voltage (\(V_{DD}\)) and the ground instead of a single transistor. As a result, the intermediate nodes of the transistors have a voltage drop, which reduces the gate-to-source voltage of the transistors that are supposed to be off. This reduces the leakage current because it becomes difficult for the current to flow through the transistors when they are supposed to be off. In addition, transistor stacking reduces gate-induced drain leakage current. Transistor stacking is effective in SRAM and logic circuits because it reduces leakage current [8], [11].

4.3 Adaptive Body Biasing (ABB)

Adaptive Body Biasing is a technique used to manage leakage currents and enhance performance in modern CMOS-based digital circuits. The technique involves adjusting the body voltage of a transistor. The body of a MOSFET is dynamically biased based on various operating conditions, including temperature, supply voltage, or workload. The threshold voltage of a transistor can be reduced or increased by applying a forward or reverse body bias. The increase in threshold voltage reduces leakage currents when the circuit is idle, which reduces power consumption. The decrease in threshold voltage increases performance when the circuit is busy [12], [13].

ABB is used to enhance performance in low-power SRAM cells, microprocessors, and other scaled CMOS-based digital circuits. The technique is used to manage leakage currents. The increase or decrease in threshold voltage is achieved by applying forward or reverse body bias. The increase in threshold voltage reduces leakage currents when idle, which reduces power consumption. The decrease in threshold voltage increases performance when busy [4], [14].

4.4 Multi - Port and 8T/9T Cells

Multi-port SRAM cells and 8T/9T SRAM cells are new SRAM cell designs with the intention of boosting the performance, stability, and leakage of the SRAM cell. In the traditional 6T SRAM cell, there is only one read/write port. In the new multi-port SRAM cell, there are read/write ports. This enables simultaneous read/write operations. The new SRAM cell has the capability to perform simultaneous read/write operations, thus boosting the performance of the SRAM cell. In the 8T/9T SRAM cell, the traditional 6T SRAM cell is modified by the addition of extra transistors. The extra transistors are used to boost the read/write performance of the SRAM cell. The use of extra transistors boosts the read performance of the

SRAM cell by reducing the leakage current. The comparison of the SRAM cell types is as depicted in table 1.

Table 1. Comparison of SRAM cell types and features

Cell Type	No. of Transistors	Read/ Ports	Leakage Reduction	Stability Improvement
6T	6	1	Moderate	Standard
8T	8	1 read, 1 write	High	Better read stability
9T	9	1 read, 1 write	High	Very good read stability
5T	5		Low–Moderate	

4.5 Power Gating and Hybrid Techniques

If the block is not in use, the sleep transistors are turned off, which is like cutting the leakage path. In the case where power gating is not effective because it has a high impact on leakage reduction, there are hybrid methods of reducing leakage. These methods include the use of transistor stacking, adaptive body biasing, or high threshold voltage [8], [19], [20]. The hybrid methods offer a better balance of leakage reduction, performance, and area efficiency, thus offering a high potential for SRAM cells and other memory cells in sub-30 nm CMOS technology, where performance and power efficiency are of great importance. The Leakage reduction techniques in SRAM as shown in table 2.

Table 2. Leakage reduction techniques in SRAM

Technique	Description
Power gating	Turn off power to the entire cell
Sleep transistors	Add transistors to cut off supply
Dynamic V_{dd}	Lower the supply voltage during standby

5. Stability and Performance Evaluation Metrics

The stability and performance of SRAM cells are of significant importance when designing sub-30 nm CMOS-based digital circuits, as leakage currents can impact reliable operation. The key performance metrics used to evaluate an SRAM cell are Static Noise Margin, Read/Write Margin, and Data Retention Voltage. The static noise margin is a measure of how an SRAM cell is able to resist disturbances during read and hold operations. The static noise margin is usually represented as the maximum square that can fit inside the voltage transfer characteristics of cross-coupled inverters [3], [7]. The read/write margins indicate how easy it is to read or write data without data corruption. The higher the margins, the better the stability of an

SRAM cell [1], [2]. The data retention voltage is a measure of the minimum voltage required by an SRAM cell to retain data. The performance of an SRAM cell is also evaluated based on its access time and power consumption. The performance of an SRAM cell is considered efficient if leakage is low and read/write speed is fast [16], [17]. The performance metrics summary is as shown in table 3.

Table 3 – Performance Metrics Summary

Metric	Description	Importance	Referen
SNM	Cell robustness against flipping	Cell robustness against flipping	[3], [7]
DRV	Min supply voltage for standby	Min supply voltage for standby	[9], [10]
ad Margin	Tolerable voltage fluctuation duri-ng read	Ensures correct read	[1], [2]
rite Margin	Tolerable voltage	Ensures correct write	[1], [2]

- Static Noise Margin (SNM): It is a measure of the cell's strength against the unintended flipping of stored data during read and hold operations. SNM is usually evaluated using butterfly curves to display the cell's strength window [3], [7].
- Data Retention Voltage (DRV): The lowest voltage required to support the SRAM cell in storing data during standby mode. Lower DRV is desirable for power-constrained applications [9], [10].
- Read and Write Margins: They are used to specify the allowed voltage variations during read and write operations. Larger margins are desirable to ensure reliable operations and are critical when scaling the supply voltage for power optimization [1], [2].

By analyzing these metrics, designers can optimize SRAM cells to achieve a balanced trade-off between stability, speed, and low-power operation, ensuring reliable functionality in scaled CMOS technologies [16], [17].

6. Conclusion

This review has highlighted the critical techniques and metrics for designing low-leakage, high-performance SRAM cells in sub-30 nm CMOS technologies. Techniques such as transistor stacking, adaptive body biasing (ABB), multi-port and 8T/9T cell architectures, and power gating/hybrid methods effectively reduce leakage current while maintaining reliable read/write operations. Evaluation metrics like Static Noise Margin (SNM), Data Retention Voltage (DRV), and read/write margins are essential for assessing cell stability and performance under process variations and voltage scaling. By combining these leakage reduction strategies with careful performance evaluation, designers can achieve SRAM cells that balance power efficiency, speed, and robustness, making them suitable for modern high-density memory applications. The continued exploration of these techniques is vital for future ultra-low-power, high-speed memory designs in advanced CMOS nodes [1], [2], [8], [16], [17], [21], [22]

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