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BROADBAND STACKED DRIVER IN SIGE:C130 NM BICMOS TECHNOLOGY FOR HIGH SPEED OPTICAL TRANSCEIVERS

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Abstract

In this work, design and simulation of a broadband stacked distributed power amplifier in SiGe:C BiCMOS 130nm technology, is presented. The proposed broadband stacked distributed driver amplifier (SDDA) consists of a unit–stack implemented in distributed topology. The SDDA deploys four sections of unit–stacks with each unit–stack comprising of three devices in the stack. The unit stack is responsible for generating large output voltage swings at the top of the stack while the device sizes in the stack are kept same in order to have same increment in the output impedance. The uniform distributed topology is preferred to implement the SDDA. Small-signal simulations of the proposed design demonstrate more than 120GHz of bandwidth with minimum of 19dB gain throughout the band. The input and output return losses are better than 7 dB. Further, only ±4 group delay variation is simulated throughout the driver bandwidth. Simulations show that the total harmonic distortion (THD) of 10% is achieved close to the saturated output power level of the SDDA. The time-domain performance of the SDDA has been evaluated through eye diagram simulations with pseudo-random binary sequence (PRBS). Simulated eye diagrams suggest an operation with open eye diagrams up to 200Gbps with driver biased under supply voltages of 4.5V.

1. INTRODUCTION

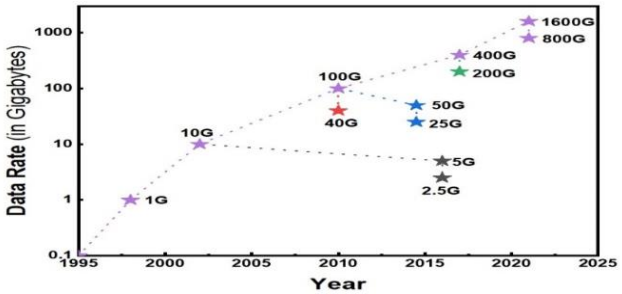

Figure 1: Recent trends for high speed data rates

Since the advent of internet, there has been an ever increase in internet—data—traffic to address a variety of bandwidth hungry applications such as high definition video, cloud enabled services, artificial intelligence based applications etc. With 400G Ethernet standardization done in 2017 [1], current focus includes 800G with advancements towards 1.6 Terabits per second in near future are foresighted Figure 1. Such stringent data rate requirements can only be met through high speed data centers where a minimum speed of 200 Gigabit per second per lane is necessary for economically feasible products. This necessitates the development of high—performance, high—speed communication optical links. Optical transceivers are a pivotal part of such high speed links, be it optical receiver front-end that includes photo—diode followed by a transimpedance amplifier (TIA) or transmitter front-end that consists of a driver and optical modulator. High speed optical transmitters do not appear as the bottleneck mainly due to the availability of high speed Machzehnder modulators and corresponding drivers as well. The major goal is to ensure a high speed driver amplifier capable of delivering large 3dB bandwidth to support 200 Gigabit per second of data rate. As per Sackinger [2], the bandwidth of the driver should be about 70% of the required data rate for a good compromise between bandwidth, output power and linearity. Thus, the driver amplifier should offer 3dB bandwidth of 120G to 140G in order to support data rate of 200 Gigabit per second per lane, should the simple case of OOK modulation is considered. Meanwhile, the SG13G2 technology from Institute for High Performance Microelectronics (IHP) offers devices with significantly higher transit frequency (f_t) and oscillation frequency (f_{max}). Therefore, a driver topology is required that should have the ability to provide the required output power over the 3dB bandwidth. This work focuses on the design of an integrated broadband driver amplifier in SG13G2 technology. The distributed amplifier topology (DA) addresses this challenge by using artificial transmission lines to absorb the parasitic capacitances of active devices, preventing gain roll-off and enabling extremely wide bandwidths. In a conventional DA, a series of gain cells are connected along input and output transmission lines, with their contributions coherently adding at the output. This allows distributed amplifiers to maintain flat gain and excellent linearity across multi-octave spans of bandwidth. However, classic DAs suffer from an inherent limitation: each gain cell operates from a relatively low supply voltage and hence generating limited output power constrained by device breakdown and current-handling capability. Non—uniform DAs are utilized to enhance the gain by removing the idle—drain line terminations [6—10], however the bandwidth obtained is limited since it is not easy to maintain broadband match without a termination.

Stacked distributed topology has emerged as an effective architecture for obtaining high output power over wideband of operation [10][14]. Conventional distributed amplifiers suffer from limited output power capability due to the voltage and current constraints of individual transistors. The stacked DPA architecture addresses this limitation by vertically stacking multiple active devices so that each device shares only a portion of the total voltage swing. This allows the amplifier to operate from a higher effective supply voltage without exceeding device breakdown limits, enabling significant enhancements in output power and power-added efficiency while preserving the intrinsic broadband behaviour of distributed structures [11—13].

By combining the high-voltage handling of stacked transistor chains with the linear, wideband gain characteristic of the distributed topology, stacked DPAs provide a compelling solution for next-generation communication and sensing systems that demand multi-octave bandwidth, compact integration, and robust power performance [20][21][23]. These amplifiers are especially well-suited for advanced CMOS and SiGe BiCMOS technologies where device breakdown limits are low and efficient power combining is challenging [28—31]. Therefore, this work describes the design and analysis of a broadband stacked distributed power amplifier in SG13G2 technology.

2. OPTICAL MODULAOR and PROPOSED DRIVER DESIGN

Monolithically integrated driver and Machzehnder modulator (MZM) comprising the linear driver and segmented depletion–type MZM have already been presented in [3–5]. The linear driver is a key component for coherent communication systems, allowing the use of high-order modulation formats. Moreover, it enhances the feasibility of applying pre–emphasis for the correction of MZM nonlinear transfer function. As discussed earlier, the most vital requirement for the driver is to produce high enough output power to drive the MZM segments. The output power directly relates to the V_{π}*L of the MZM, where V_{π} is the voltage required to induce π phase shift for a length of the MZM segment. This implies that in order to get larger phase modulation from the MZM segment, the driver should generate larger output swings and hence output power. An MZM segment along with driver have been depicted in Figure 2. Rn and Rp represent the series resistances of the highly doped section whereas Cpn represents the reverse biased capacitance. The voltage swing of V_{π} is established across the reverse biased junction that induces the phase shift in optical signal through the refractive index.

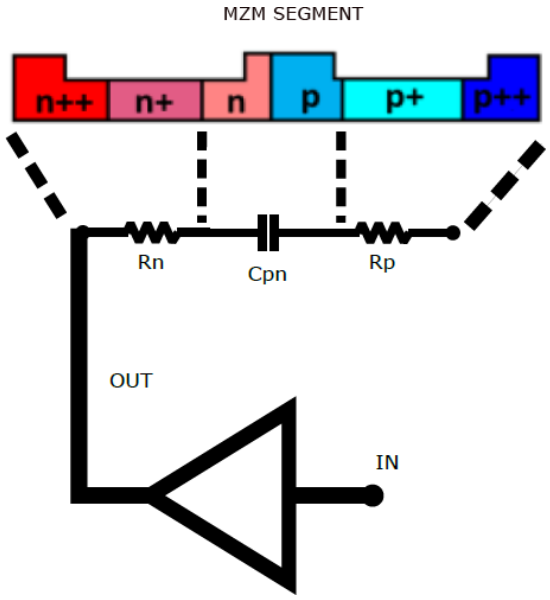

Figure 2: Driver and Machzehnder modulator segment

For a conventional distributed amplifier, the input–output artificial transmission lines are formed by the shunt parasitic capacitance and the series inductors. To maximize the signal addition at the output of each gain cell, the phase velocities of both the lines are matched while their characteristics impedance is design to be 50Ω to ensure match at the input–output ports [17–19].

A. UNIT-STACK

Stacking principle allows a number of transistors stacked on top of each other to produce high output voltages. Practically, the actual number is limited by a number of factors pertaining to the technology utilised. For instance, stacked PA implementations in standard CMOS are governed by the substrate breakdown and gate–oxide breakdown voltages [6]. This leads to maximum number of devices in stack configuration which has been three [10] and four [23–26] in the recent implementations. Same is the scenario for the BiCMOS technology where collector/emitter to substrate breakdown voltages are the limiting factors. Moreover, the biasing for such topology plays very important role for the

safe and efficient operation which turns out to be different than a conventional cascode that deploys larger capacitances to provide good groud for the AC signal [14]. In stacking, smaller capacitances at the base of the common–base devices are used that form a voltage divider with the device parasitics capacitances to allow a small AC swing and hence, effectively reducing the difference in nodes AC voltage potential. This is particularly crucial to the top most device in the stack since it experiences the highest collector–to–emitter swing and requires significant swing at the base to avoid reverse bias collector–to–base breakdown voltage. In the proposed design, three devices have been placed in the stacked configuration for a safer operation to avoid voltages breakdown. Some recent works used up to six devices in the stack but they are implemented on silicon–on–insulator (SOI) CMOS technology which extends the substrate breakdown voltages through the introduction of an insulator but is a costly solution [14][16].

Table I. Device Sizes in the Unit-Stack

Device	Sizes
Q_1	4 X 70 X 900 nm
Q_2	4 X 70 X 900 nm
Q_3	4 X 70 X 900 nm

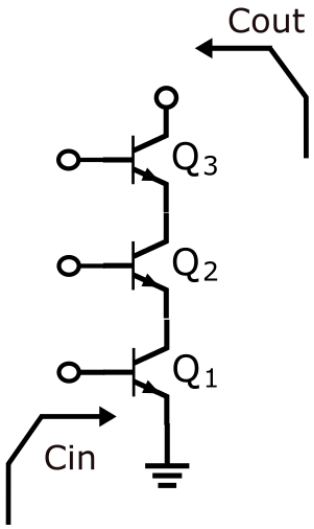

Figure 3: Unit-stack cell

The unit stack cell has been depicted in Figure 2. Three devices $Q_{1–3}$ are placed in stack configuration. The DC voltage drops across each device plus the resistor establishes the maximum DC supply voltage. Let us assume that optimum impedance seen at the collector of the Q_1 device is R_{opt} where output swing Vout (V) is produced. As we move up the stack, the impedance seen from the collector of Q_2 becomes $2*R_{opt}$ and hence, subsequent proportional increase in the output swing to 2*Vout (V). It should be noted that this two–times increase in impedance happens only if the sizes of all the devices in stack are kept same. Similarly, the output impedance and voltage swing at the collector of Q3 becomes three times the impedance and output swing at the collector of Q_1. The output voltage waveforms at the collector of each device will be shown later in following section. Thus, the overall voltage swing obtained from the stack is three times than the swing obtained from a single device. Further, the input and output capacitances need to be

analysed since they will become the shunt part of artificial transmission lines. In order to design the artificial transmission lines, the input–output capacitances of the unit–stack cell have been extracted across the frequency and are plotted in Fig. 4. The input and output capacitances are device dependant and vary around 80 fF and 20 fF, respectively. These capacitances along with the series inductances define the cut-off frequency of the artificial lines and hence the actual 3–dB bandwidth of the amplifier. Once the average value of these capacitances are known, then the next step involves design the inductor with the value that should give us the required characteristic impedance of the line which in our case is 50Ω. The device sizes are tabulated in Table I.

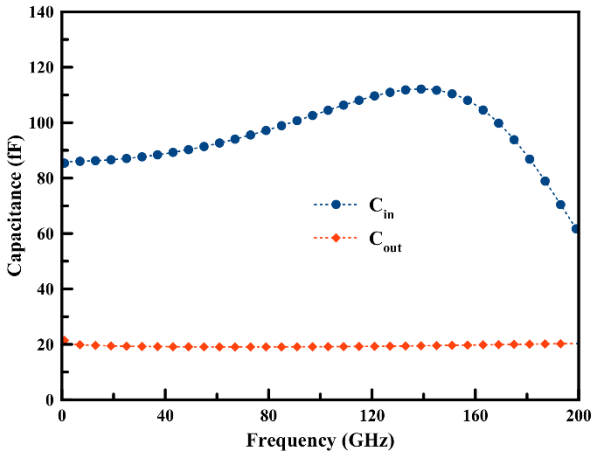

Figure 4: Input-output capacitance of the unit-stack

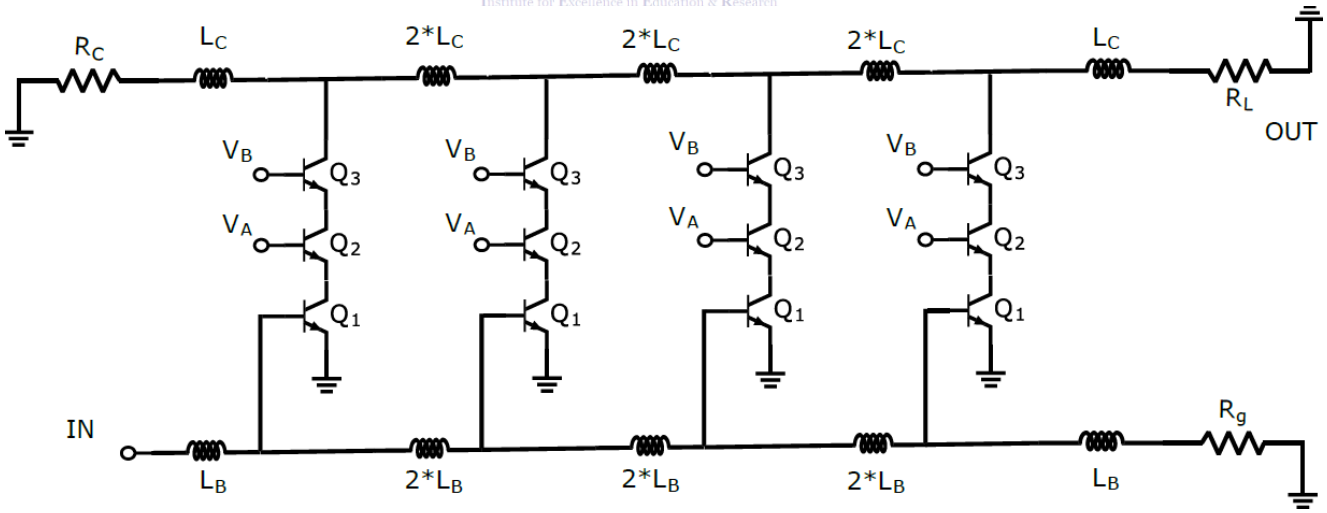

Figure 5: Copletem design of the proposed stacked distributed amplifier in IHP SG13G2 technology

3. Complete Circuit Design

The unit stack in the stacked implementation consists of three transistors. The three transistor stack offers multiple advantages such as 1) maintain the biasing conditions for each device in the stack well within the safe operation region while using a relatively low dc supply. For instance, in the proposed design three devices are biased from a drain supply of 4.5 V to have a drop of 1.2 V across each transistor and rest

across the resistor placed at the collector. The number of unit stacks in the amplifier design defines the total gain of the amplifier. The optimum number for the unit stacks is mostly limited to four. It is because of the attenuation introduced on the artificial lines that attenuates the input signal to a level that the later sections in design do not get enough excitation. In our design, four sections of unit–stacks have been deployed mainly because it provides enough small-signal gain that is around 20 dB. The other major factor in defining the maximum number of unit–stacks is the power dissipation requirement and attenuation on the line. Addition of new section implies more power dissipation and area especially when it is not contributing much in terms of gain.

The output swings at the collector of each device in the stack increases as one moves up the stack [14][16][20][23]. In order to get the maximum output voltage swing, the individual swings should add up phase. This can be controlled through the input swing established at the capacitive

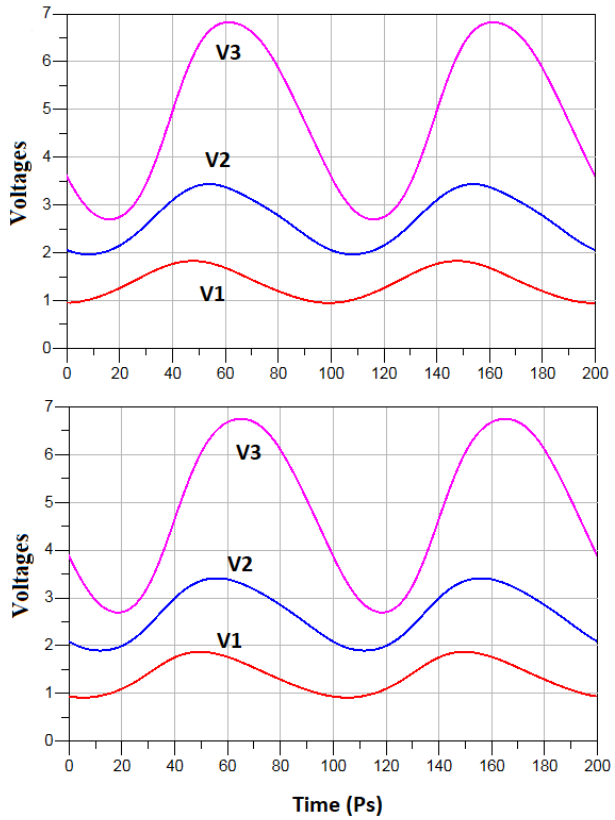

Figure 6: Voltage swings at the collector nodes of devices in the first and last unit–stacks

voltage divider and through the addition of a series inductance between the devices. Furthermore, the base series inductance L_B and collector series inductance L_C of the artificial lines should be designed to serve two purposes. Firstly, the characteristic impedance should be maintained 50Ω to ensure input–output match to external 50Ω load and secondly, the phase velocities of both the lines should be same to avoid any mismatches. This also reflects in the output voltage swings plotted at the collector nodes in the stack, also shown in Figure 6. V_1, V_2 and V_3 represent voltage swings at the collector node of Q_1, Q_2 and Q_3, respectively. As can be seen from the Figure 6, all the peaks of the $V_{1–3}$ are aligned in both, the first and last unit–stacks that reflect the phase velocities at the base and collector artificial lines. The complete schematic

of the proposed stacked distributed amplifier is depicted in Figure 5 while all the component values are tabulated in Table II.

Table II. Device Sizes in the Unit-Stack

Device	Sizes
$Q_{1\text{-}3}$	4 X 70 X 900 nm
L_B	120 pH
L_C	100 pH
L_{RFC}	10 nH
R_C	50 Ω
R_g	50 Ω
R_L	50 Ω
V_b	0.87 V
V_A	1.6 V
V_B	2.5 V
V_{CC}	4.5 V

4. Simulation Results and Discussions

The design has been characterized with three main analyses.

A. SMALL–SIGNAL SIMULATION

Small–signal simulations have been performed for the four–section stacked distributed amplifier and the results are plotted in Figure 7. The design offers more than 20 dB gain over a bandwidth of 120 GHz leading to simulated Gain-Bandwidth Product of more than 1 THz. The input and output return losses are better than 5 dB that tend to improve further once the design is realized using EM simulated inductors. The input–output isolation is better than 50 dB. The other important parameter for a broadband design is stability. Rollet stability factor is simulated for the design and the results are depicted in Figure 8. The K–factor is larger than 1 demonstrating the design is unconditionally stable over the entire operational band. This also stems from the fact that no excessive bandwidth extension technique is utilized. The simulated bandwidth originates primarily from the distributed architecture. This also reflects in the simulated group delay which is 15 *p*S with overall variation of ±5 *p*S till 100 GHz as shown in Figure 9. Such minimal group delay variation is very useful when broadband signal is applied to the design. This phenomenon can be clearly viewed through time domain performance of the SDDA show later in this section.

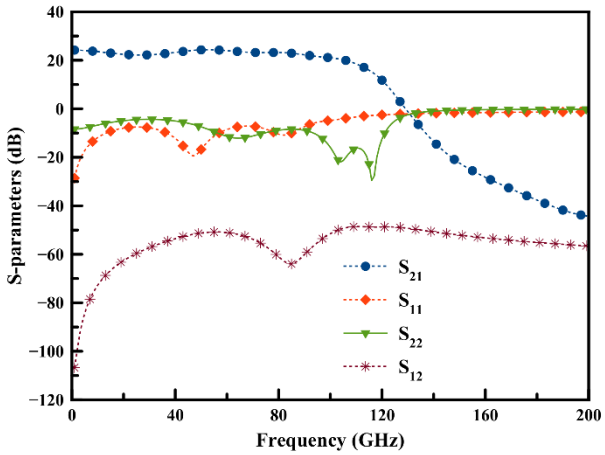

Figure 7: Simulated S-parameters of the proposed broadband stacked distributed power amplifier

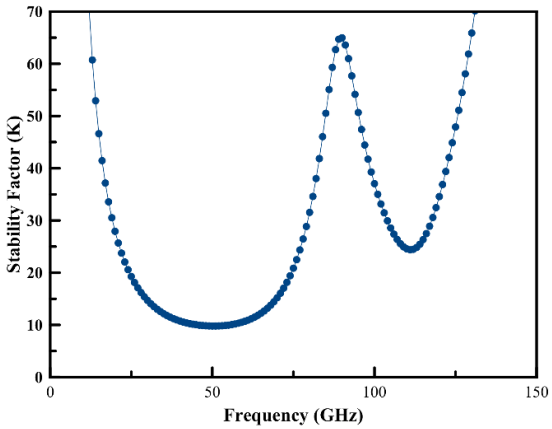

Figure 8: Simulated stability of the proposed broadband stacked distributed power amplifier

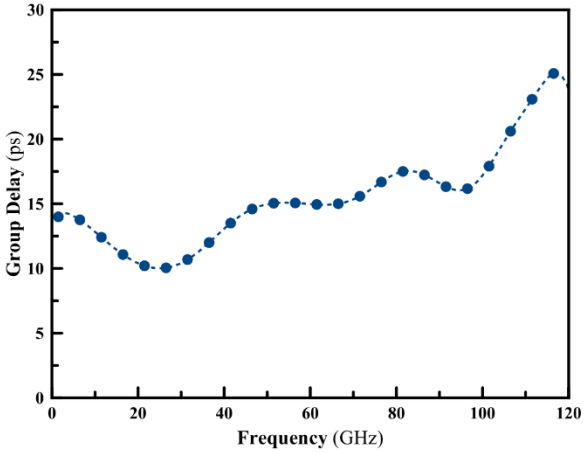

Figure 9: Simulated group delay of the proposed broadband stacked distributed power amplifier

B. LARGE-SIGNAL SIMULATION

The large-signal performance is characterized through Harmonic Balance simulations. The output saturated power versus the input power has been simulated at 1 GHz. The maximum saturated power is around 23dBm which is quite sufficient for many applications. Please note that design involves standard uniform distributed implementation that is more suitable for stable addition of currents at each node. In order to characterize the linearity of the design, total harmonic distortion (THD) is evaluated at 1 GHz. THD can be defined as

$$THD = \frac{Power\ in\ Harmonics}{Power\ in\ the\ Fundamenal}$$

The THD is 5% at an input power of −15 dBm. Meanwhile, it can also be observed that the SDDA starts to enter into saturation at that power level.

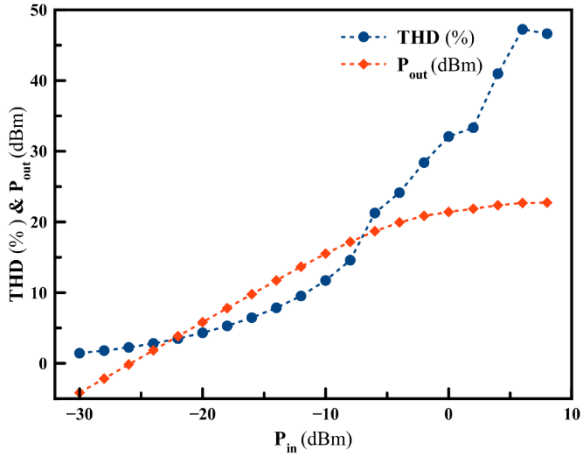

Figure 10: Simulated output power and total-harmonic distortion at 1GHz

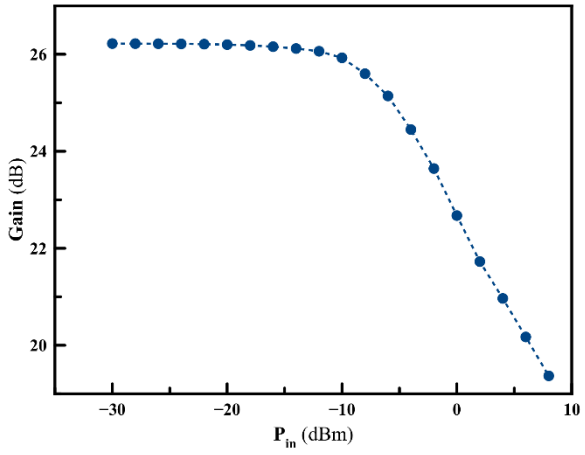

Figure 11: Simulated large-signal gain of the proposed stacked distributed power amplifier

The large–signal simulated performance of the SDDA is demonstrated in Figure 10 and Figure 11.

C. TIME DOMAIN SIMULATION

In order to simulate the time domain performance, the input PRBS sequence generated at baud rates of 100G, 160G, 200G is fed to the proposed SDDA. The input voltage applied to design is set to be 100 mVpp which lies in the small-signal range. Resulting simulated output eye diagrams are in mV and plotted in Figure [12], Figure [13] and Figure [14]. The eye diagrams are significantly open and clean at 100G and 160G. For 200G, the eye is relatively small and the jitter is around 2 psec at the maximum 200 Gb/s rate which is reasonably small for such high data rates. Subsequently, the inductive peaking deployed in the design is also optimum since clean and wide eye diagrams can be seen at 200 Gb/s of data rate.

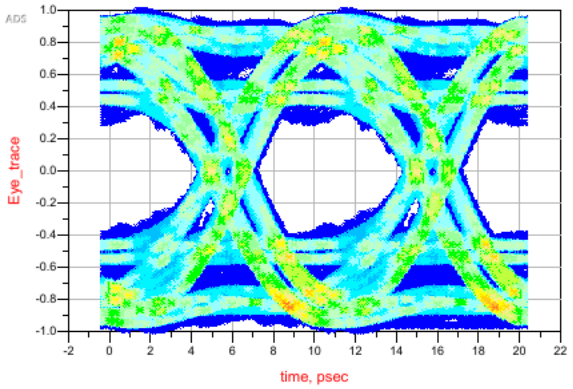

Figure 12: Simulated eye diagram at 100 G

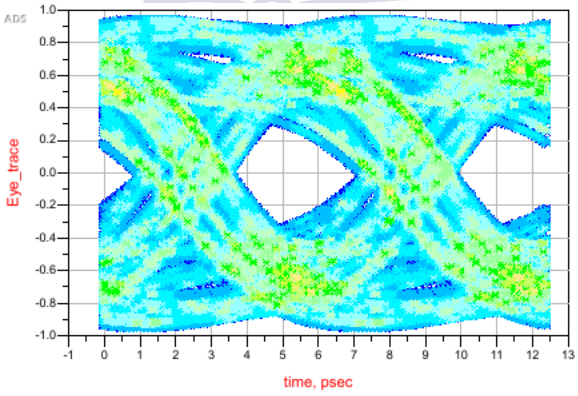

Figure 13: Simulated eye diagram at 160 G

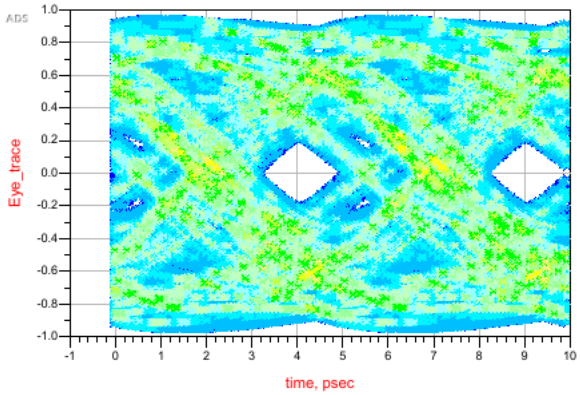

Figure 14: Simulated eye diagram at 200 G

5. CONCLUSION

This work describes a broadband stacked distributed driver amplifier with a 3 dB bandwidth over 120 GHz with a gain of 20 dB. The SDDA deploys four sections in the distributed toplogy to target large gain. Three devices in the stack ensure large swings such as the total saturated output power becomes 22dBm that corresponds 8 V Vpp to swing at 50Ω reference impedance. This swing is large enough to induce significant phase shift in the Machzehnder modulator that could potentially lead to smaller size of the MZM segment. The SDDA topology also offers reasonable linearity which is less than 10% near the saturated output power. Lastly, the time domain simulations depict a clean eye till 200 GHz which demonstrate that the proposed driver topology has the capability to be used as the high speed driver for 800G and futuristic 1.6T data centers and suffices the requirements for high speed optical transceivers.

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